

Fig 1

Transmit 201

Receive 202

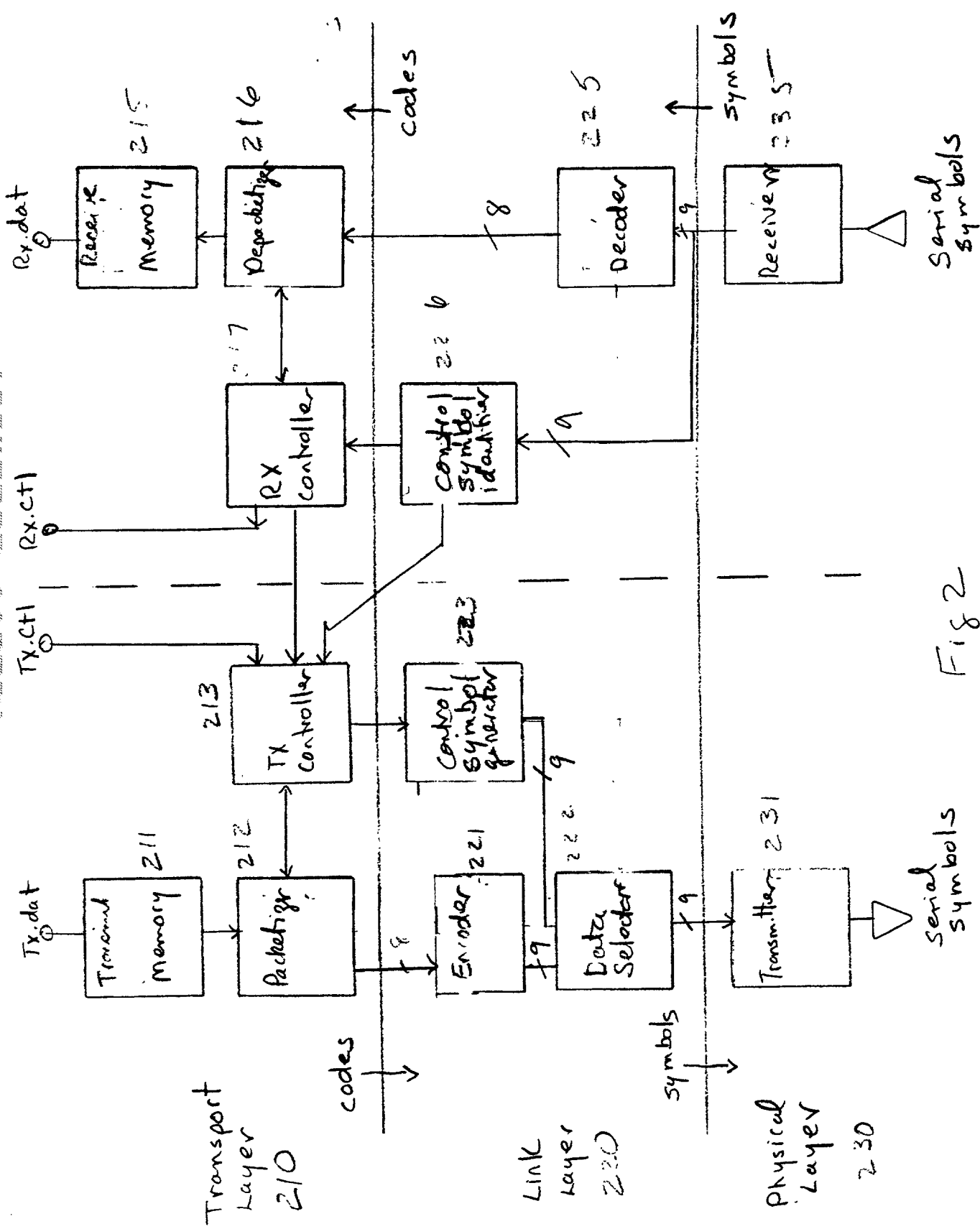


Fig 2

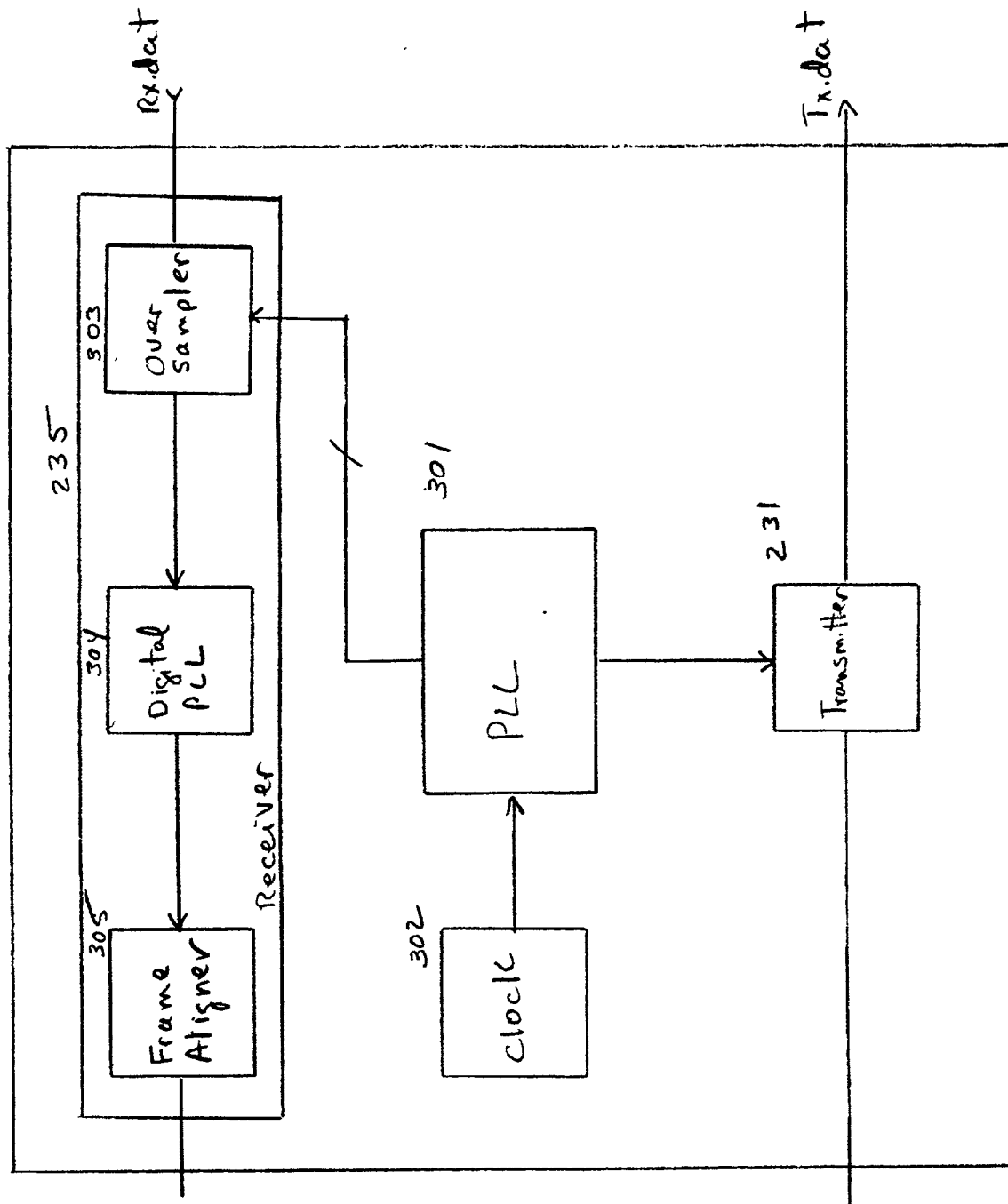


Fig 3

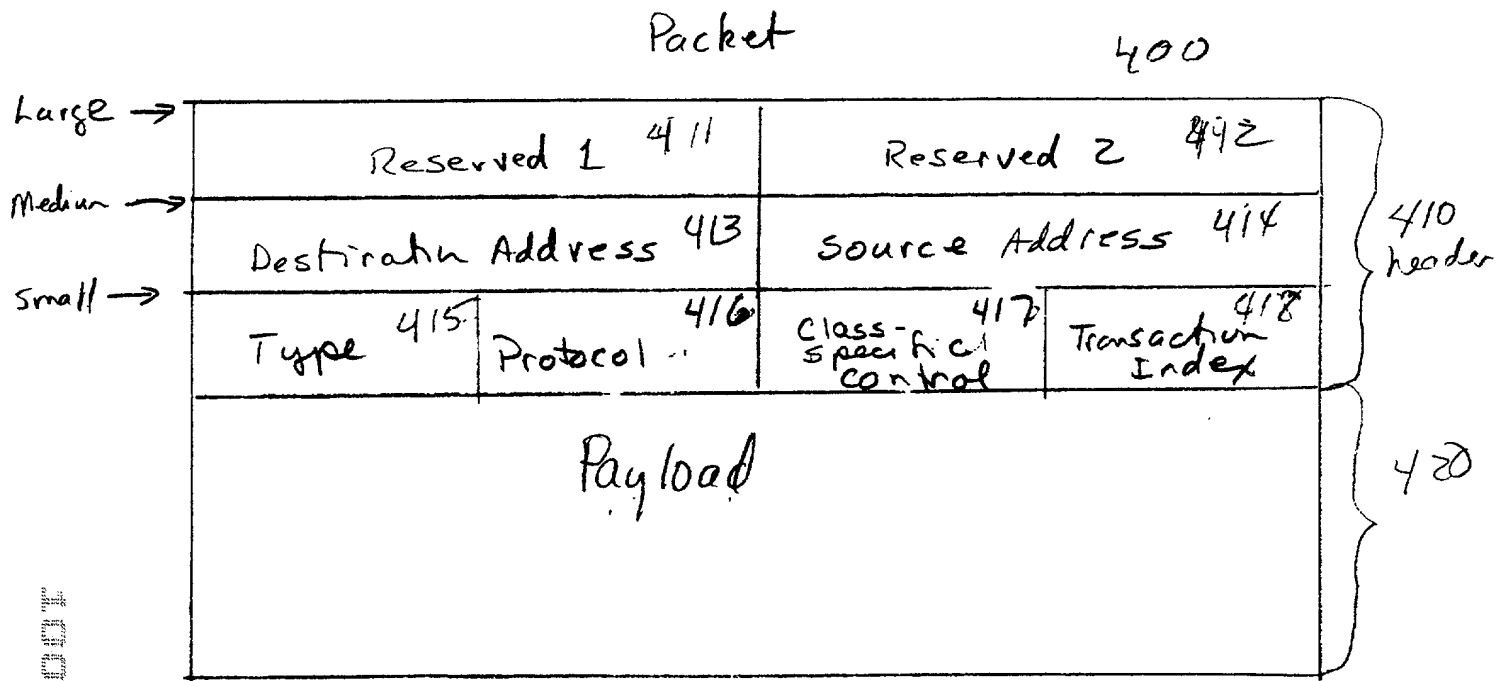
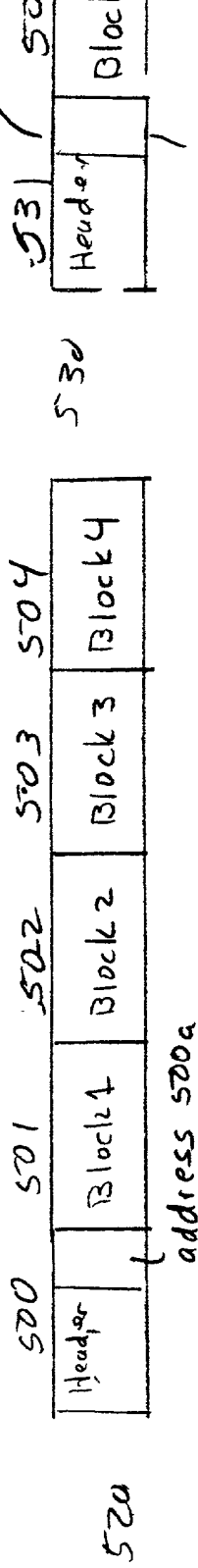
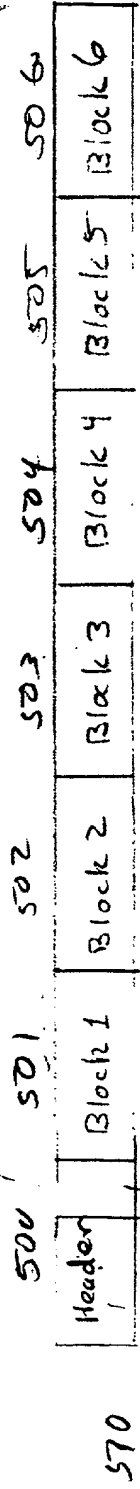


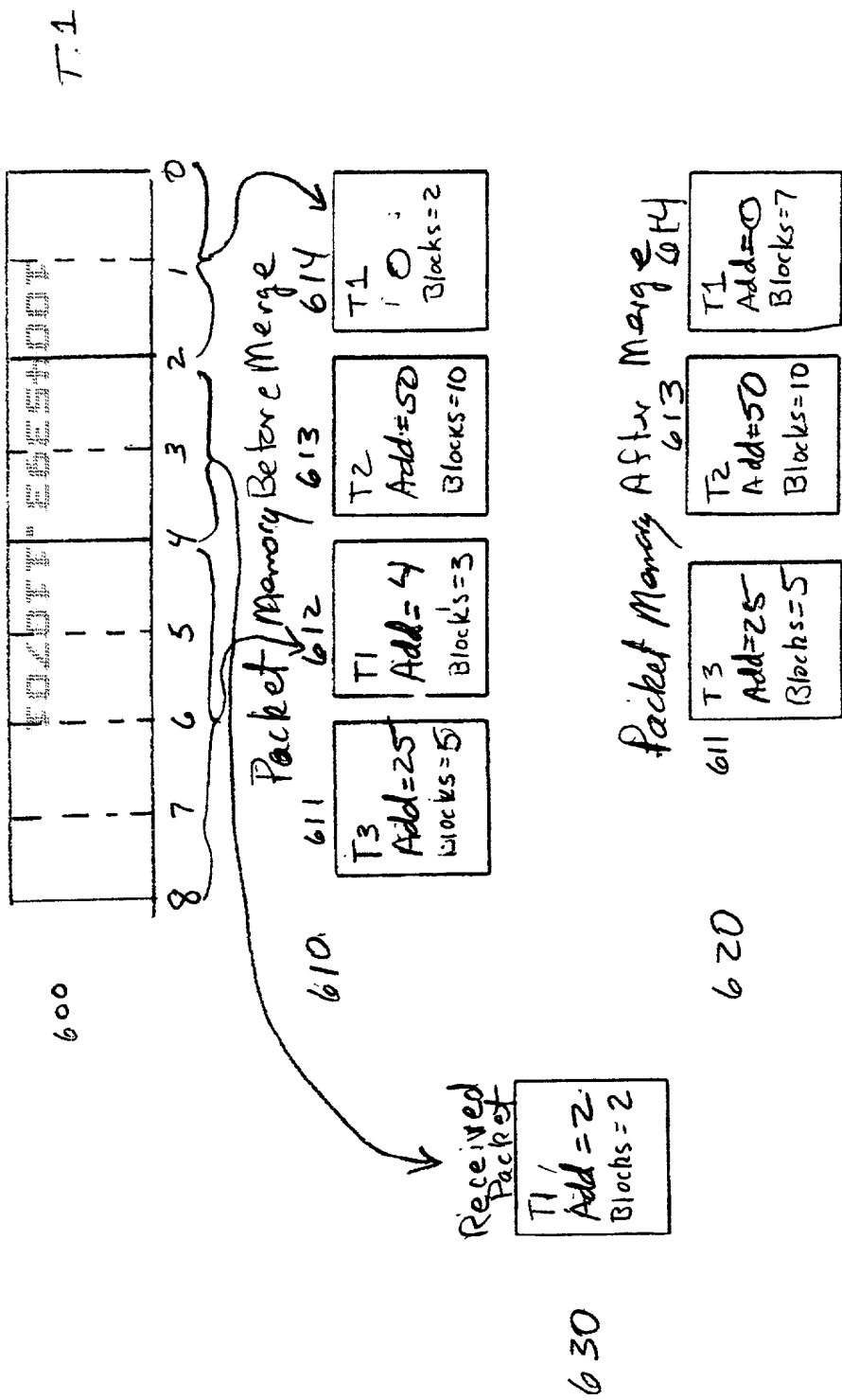
Fig 4

1004593 10704

# payload size



535



F. 86

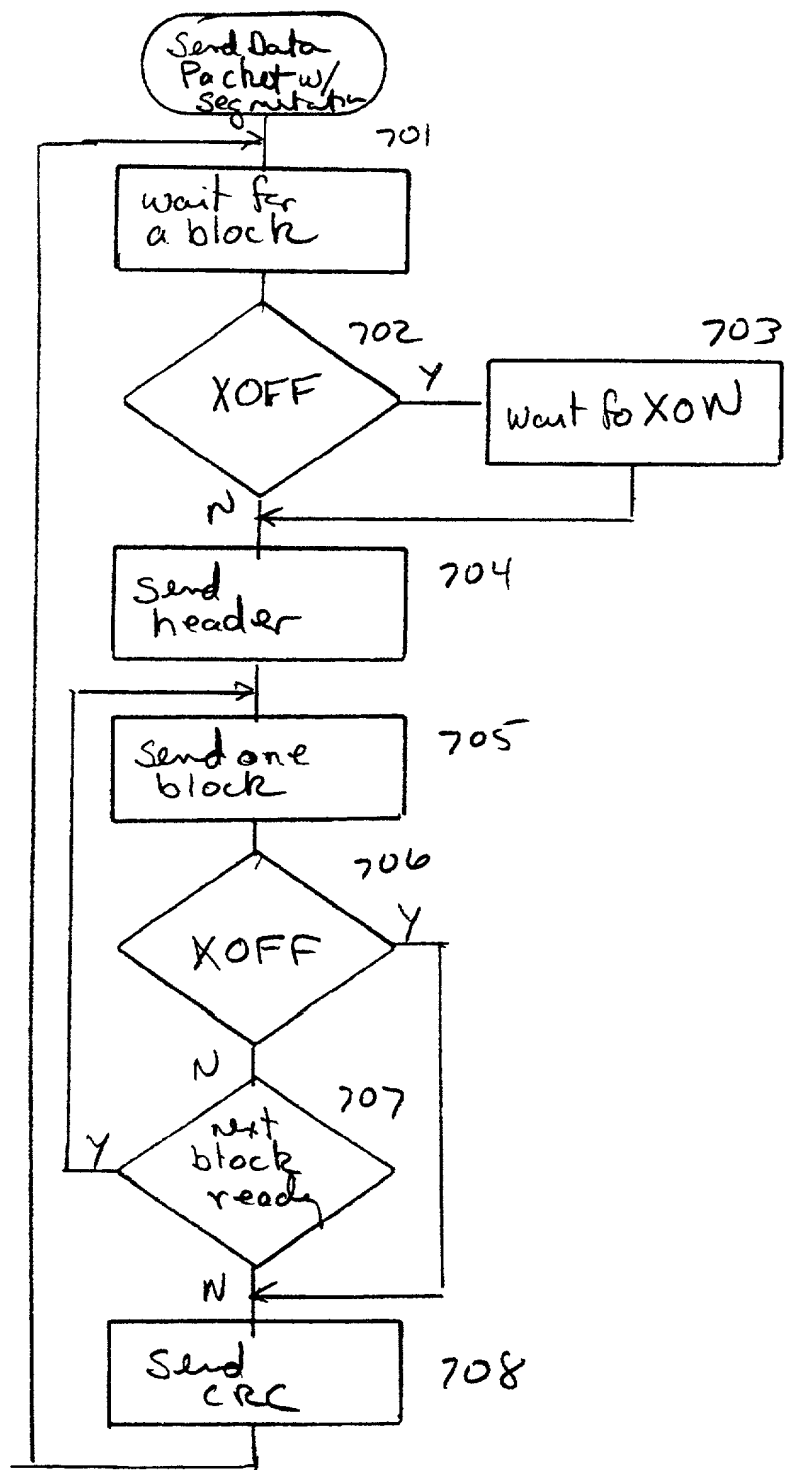


Fig 7

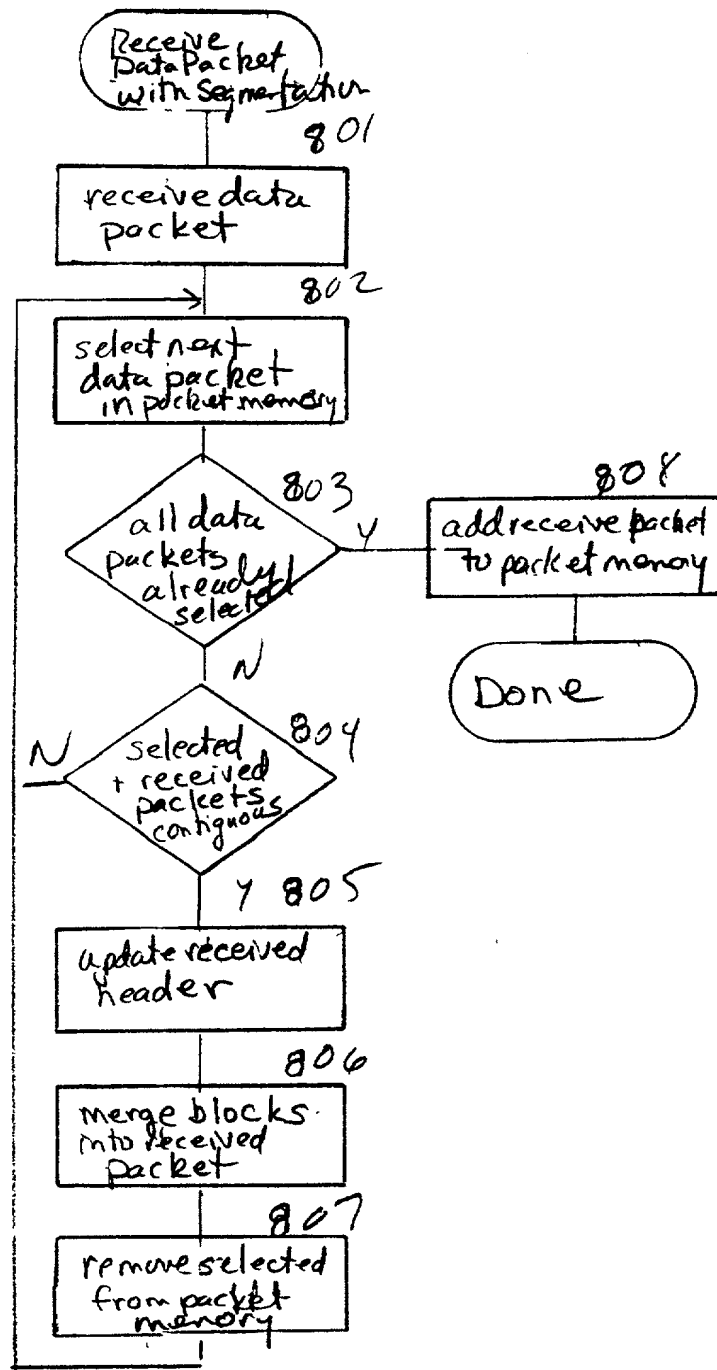
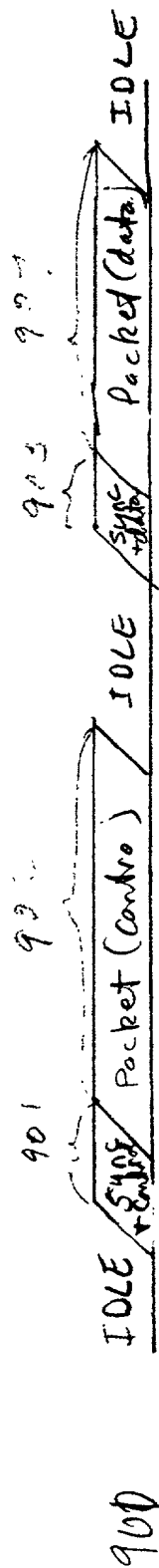


Fig 8



sync + packet type

Fig 9A

BIT BUFFER	A8	A7	A6	A5	A4	A3	A2	A1	A0	B8	B7	B6	B5	B4	B3	B2	B1	C0	C8	C7	C6	C5	C4	C3	C2	C1	C0
BIT CONTENT	0	0	1	0	0	0	0	0	0	0	1	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0
"10" DETECTION	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/	/
"10" DETECTION	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
RESULT																											
Symbol																											
STARTING POINTS																											

FIG.10

Fig 9B

910

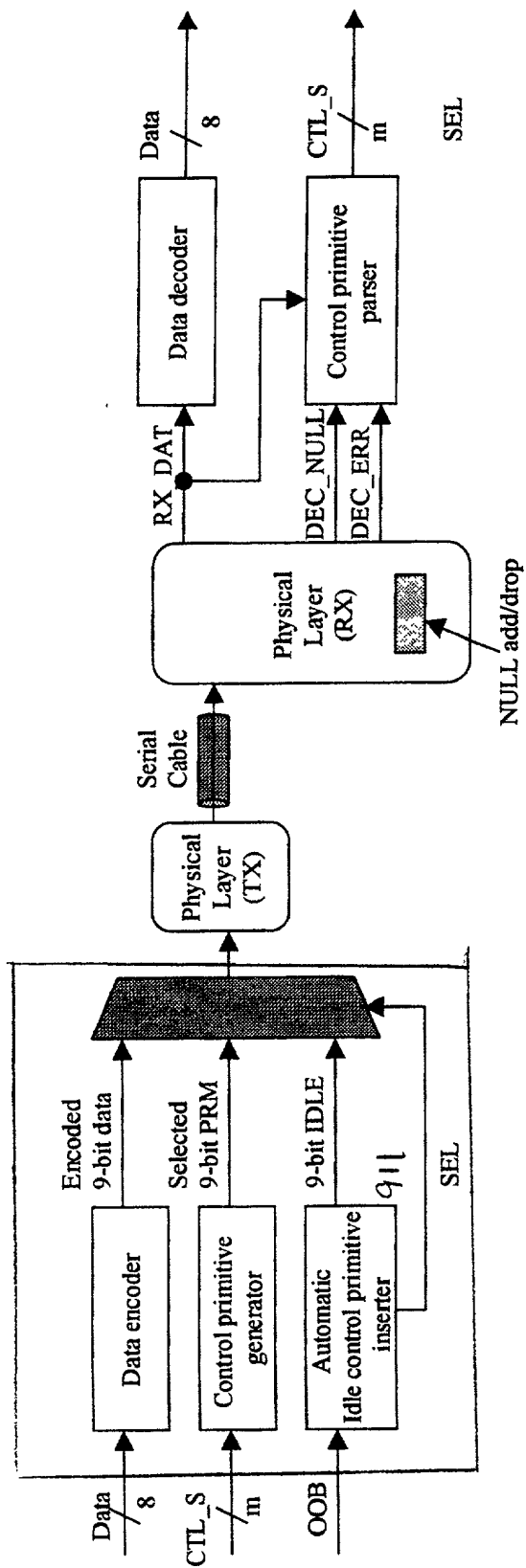


Fig. 9C

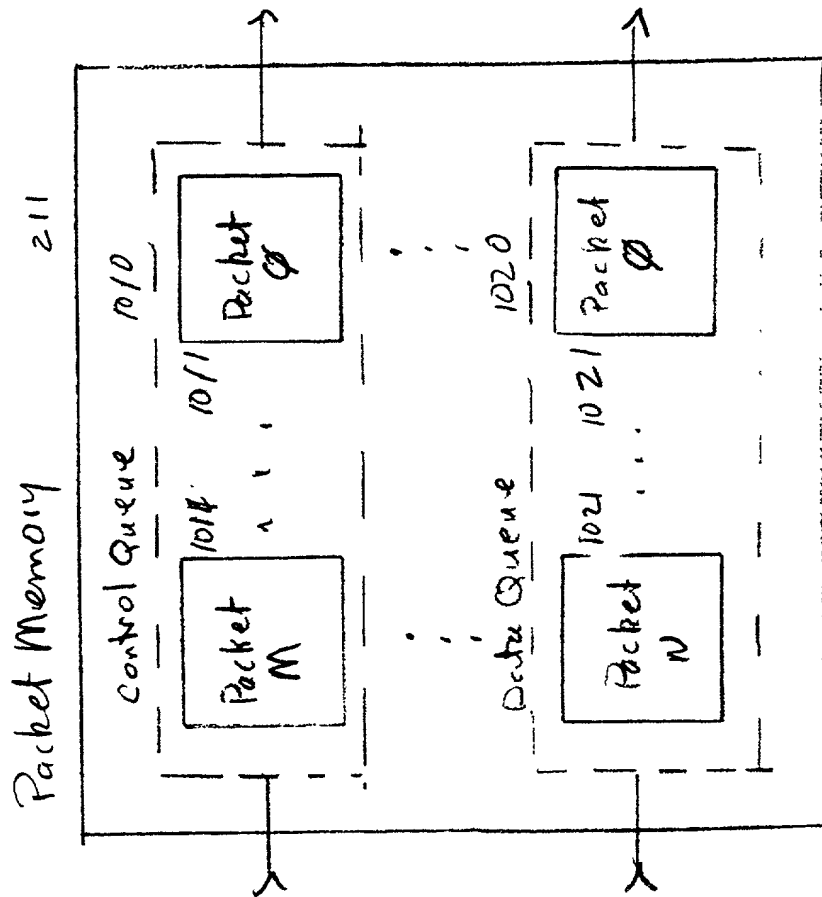


Fig 10

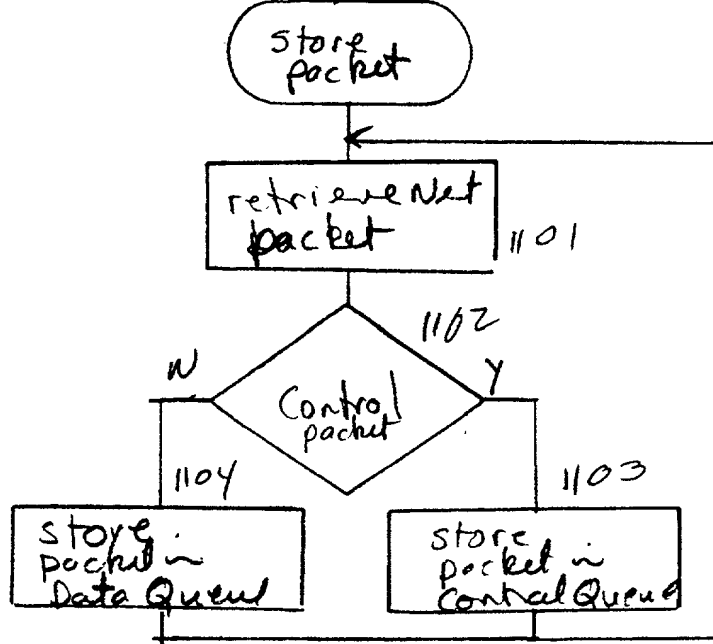


Fig 11

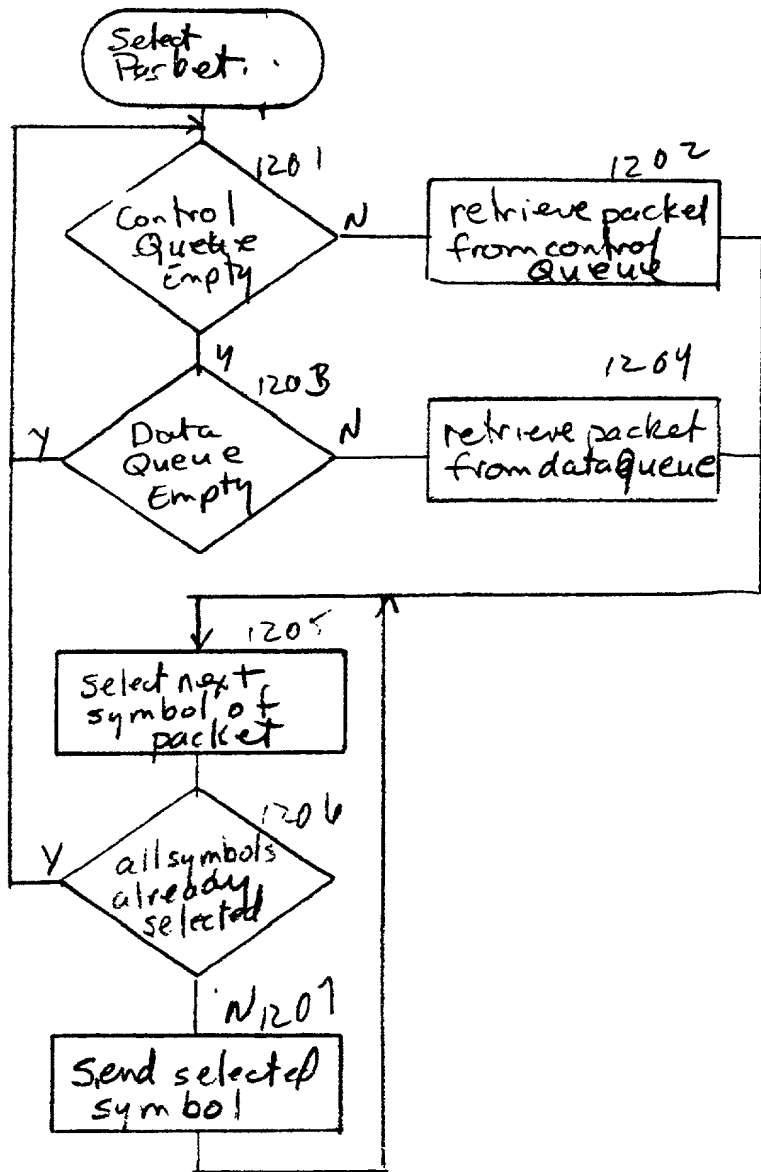


Fig 12

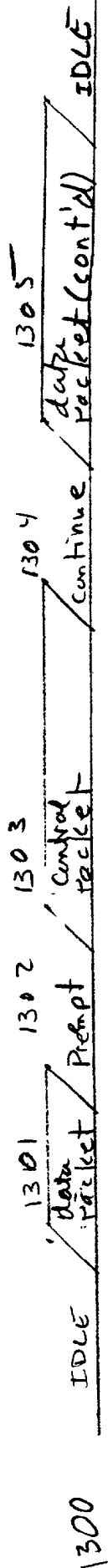


Fig 13

10045393 10001

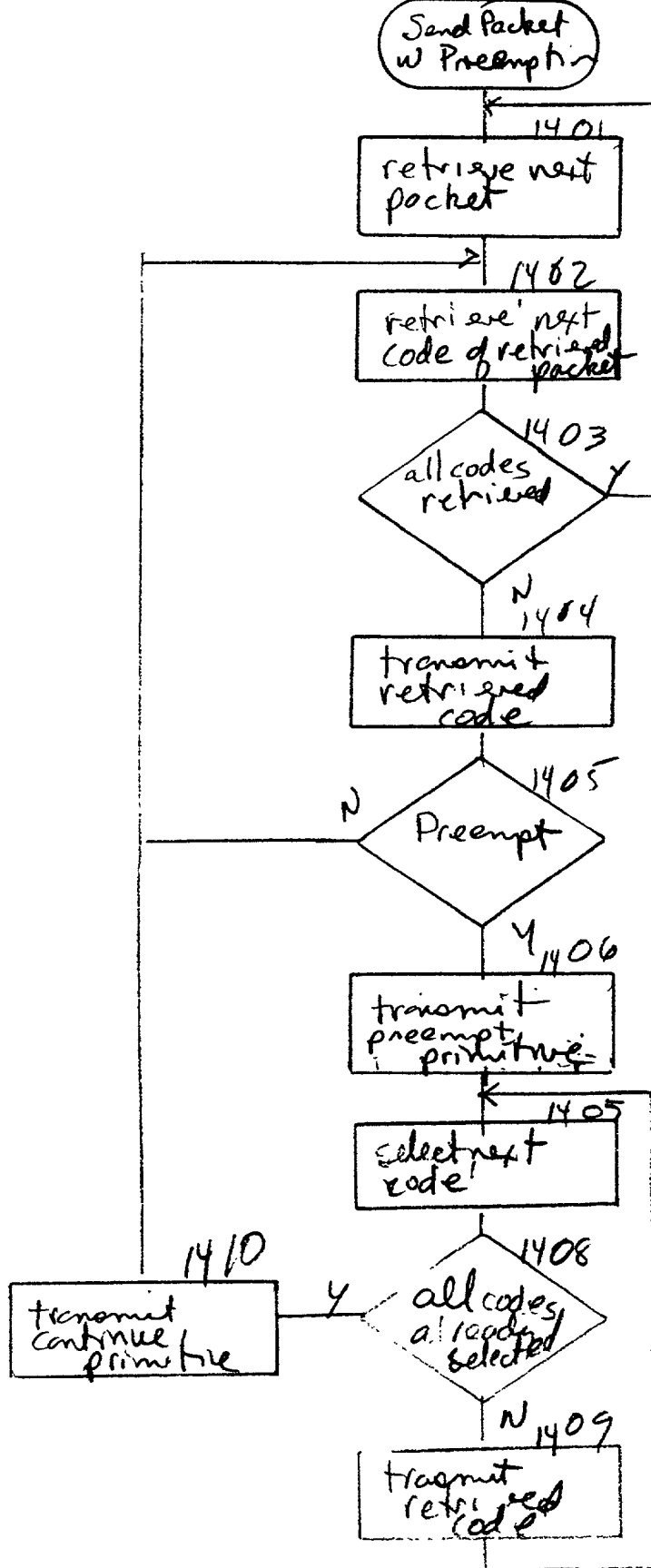


Fig 14

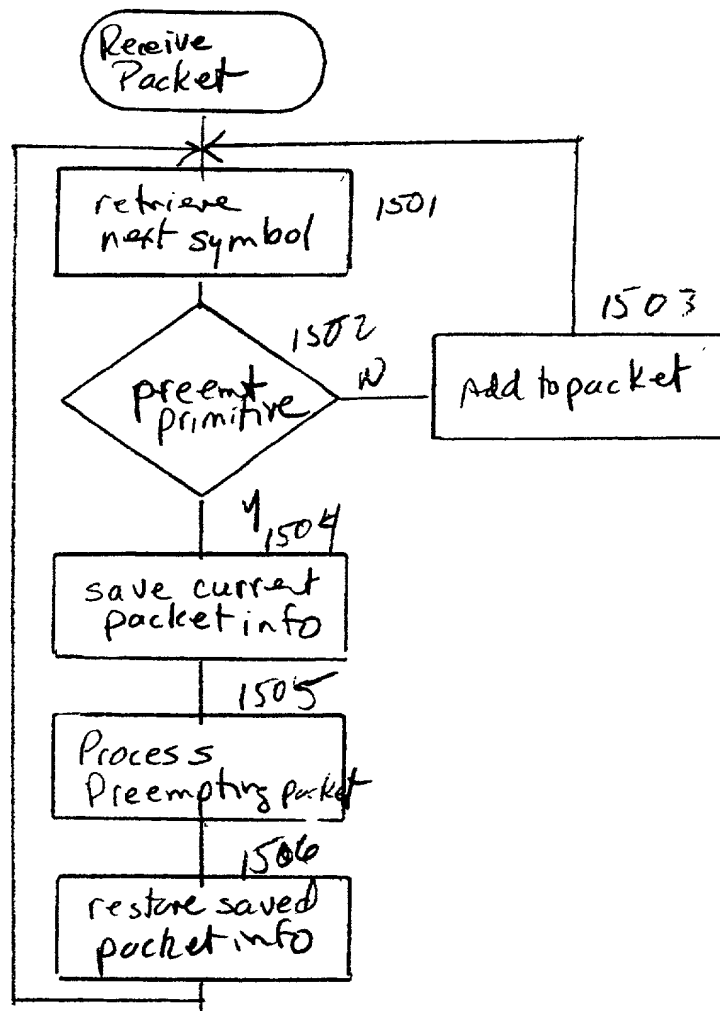


Fig 15

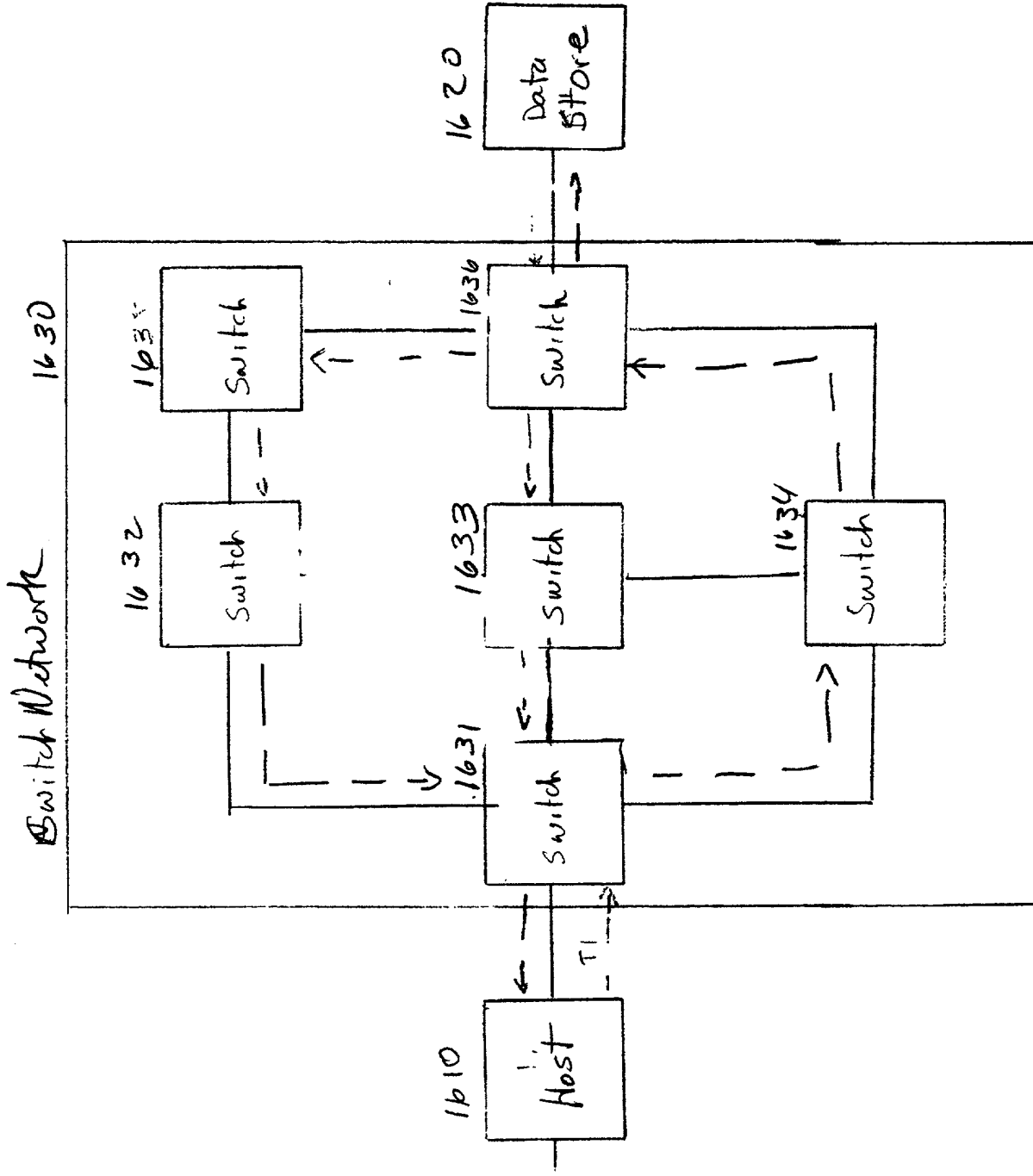
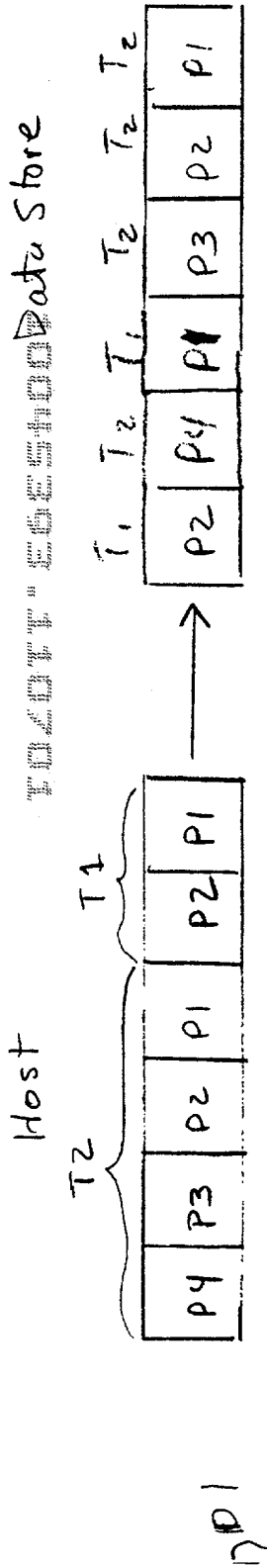
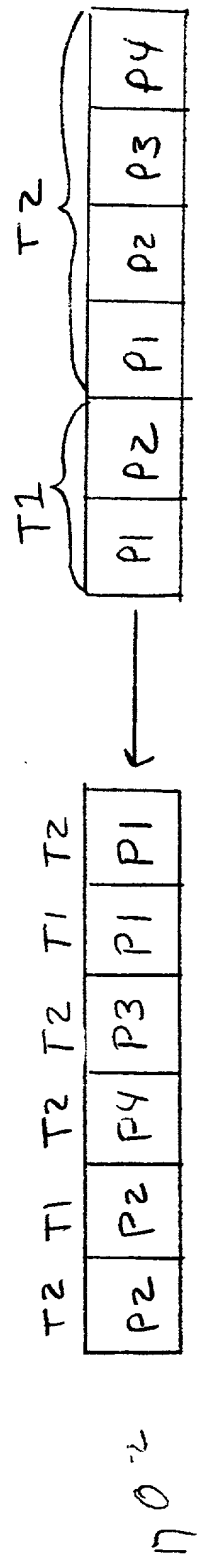


Fig 16



Preserving Packet Order w/ Transaction



No Packet or Transaction Ordering

Fig 17

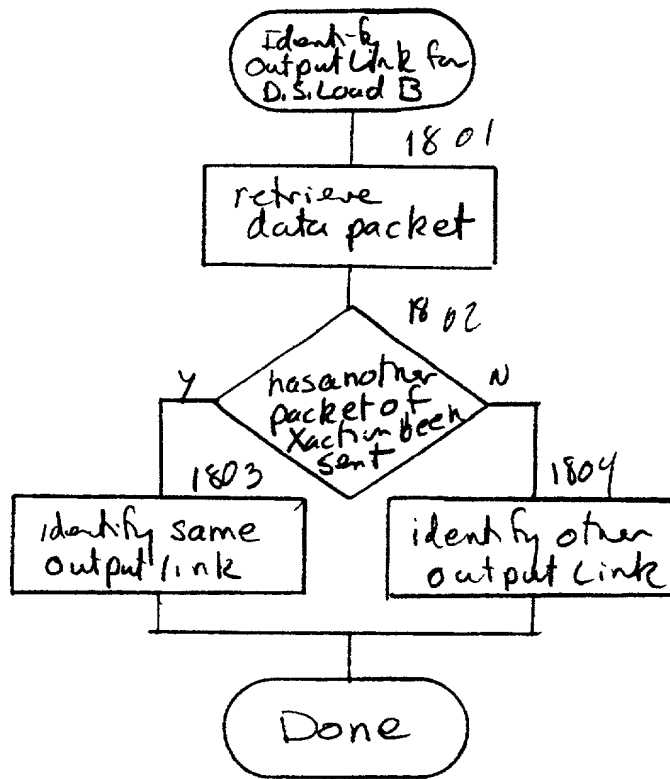


Fig 18

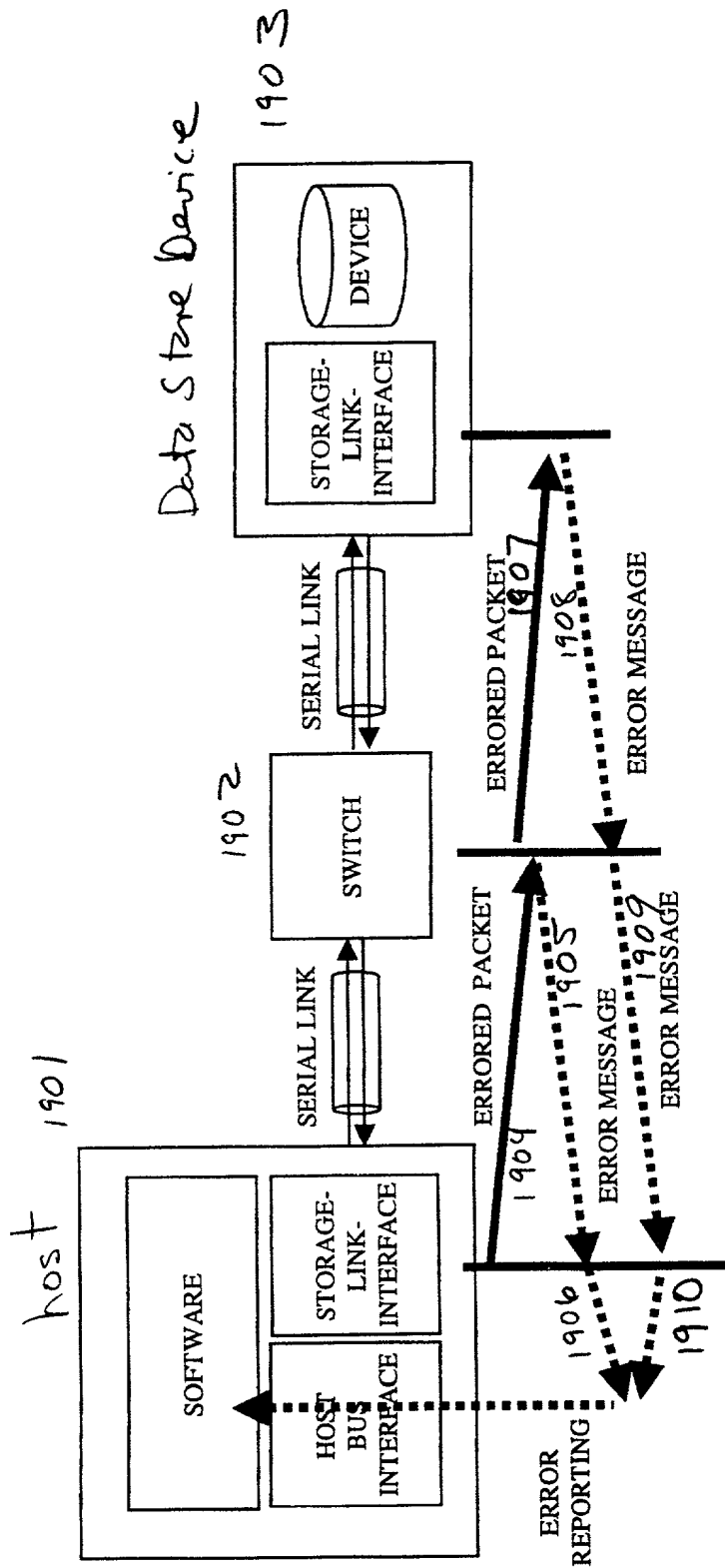
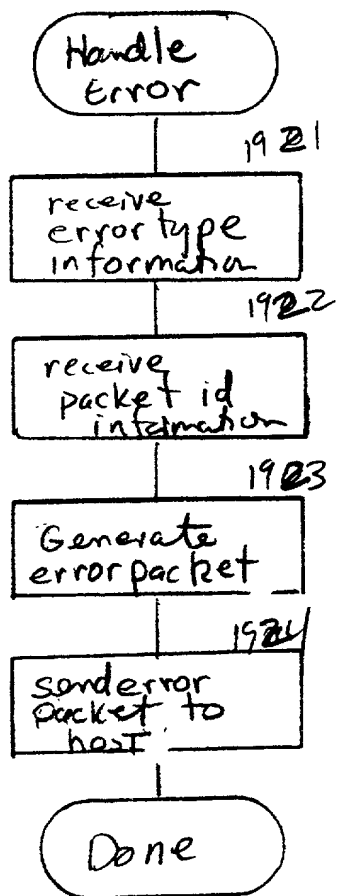


Fig 19A

1901





19C

10045303 110704

8 b Code	9 bit symbol
0 0 0 0 0 0 0 0	1 0 1 0 1 0 1 0 1
0 0 0 0 0 0 0 1	1 0 1 0 1 0 1 0 0
0 0 0 0 0 0 1 0	1 0 1 0 1 0 1 1 1
⋮	
0 1 0 1 0 1 0 1	0 0 1 0 1 0 1 0 1
⋮	
0 1 1 1 0 1 1 0	0 0 1 1 1 0 1 1 0
0 1 1 1 0 1 1 1	1 0 0 1 0 0 0 1 0
⋮	
1 1 1 1 1 1 1 1	1 1 0 1 0 1 0 1 0

Fig 20

101011001001001001

Block  
Disparity  
+4

Symbol  
1

101010101

Alternate  
Bit  
Inversion

Symbol  
2

001110110

Symbol  
3

101010101

Bit  
Inversion

Symbol  
4

110101010

00000000

110001001 010101000 001010101

Fig 21A

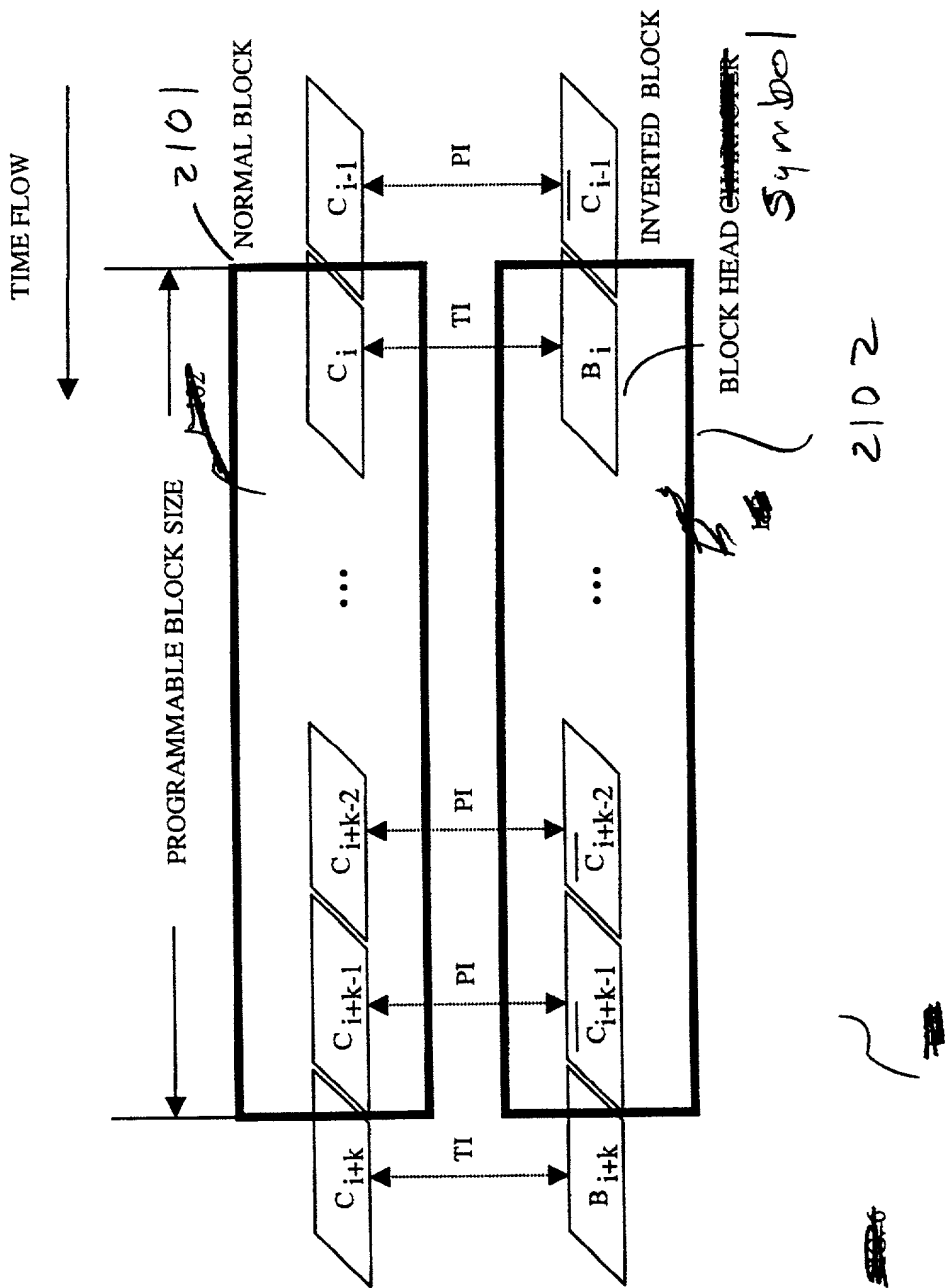


Fig 21B

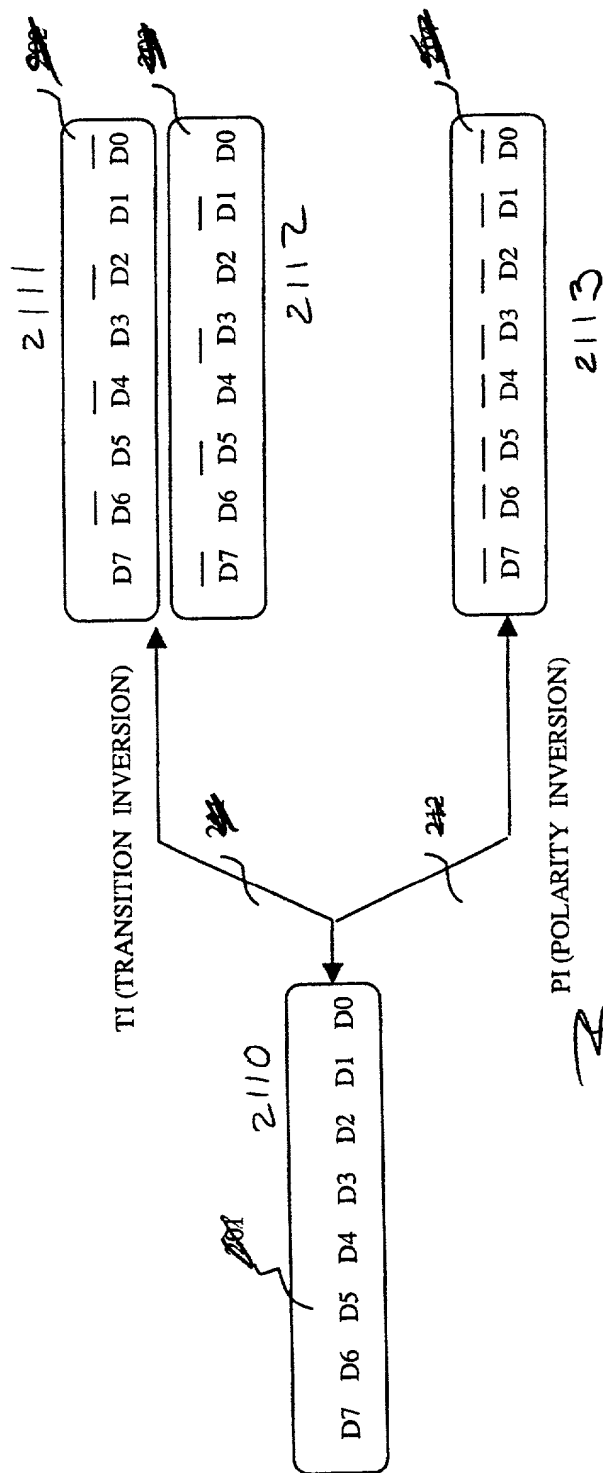


Fig 21C

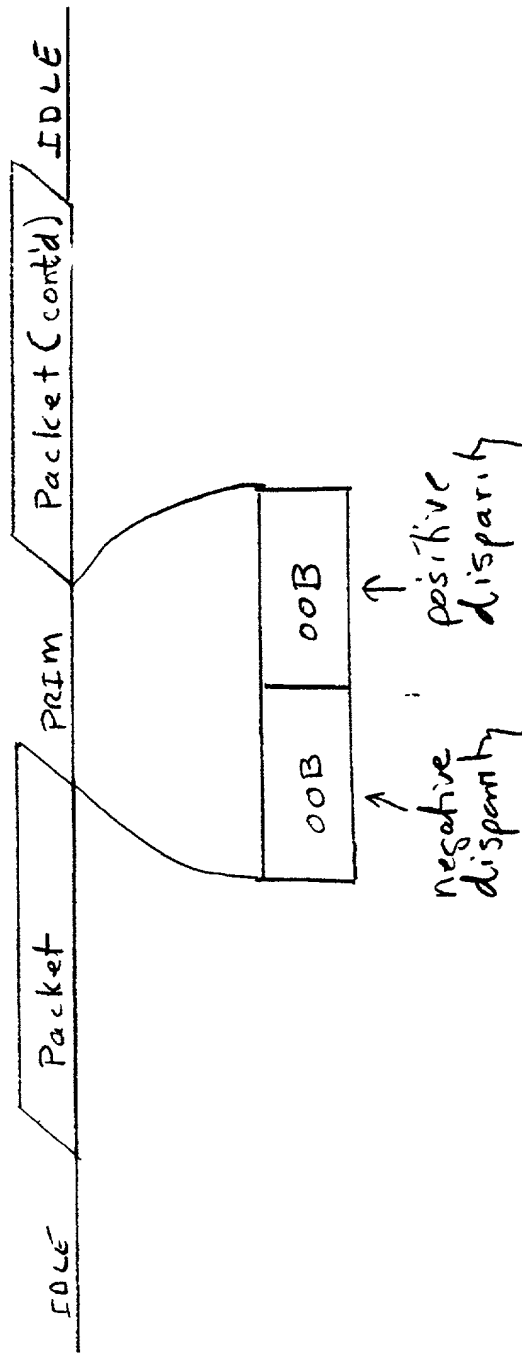


Fig 22

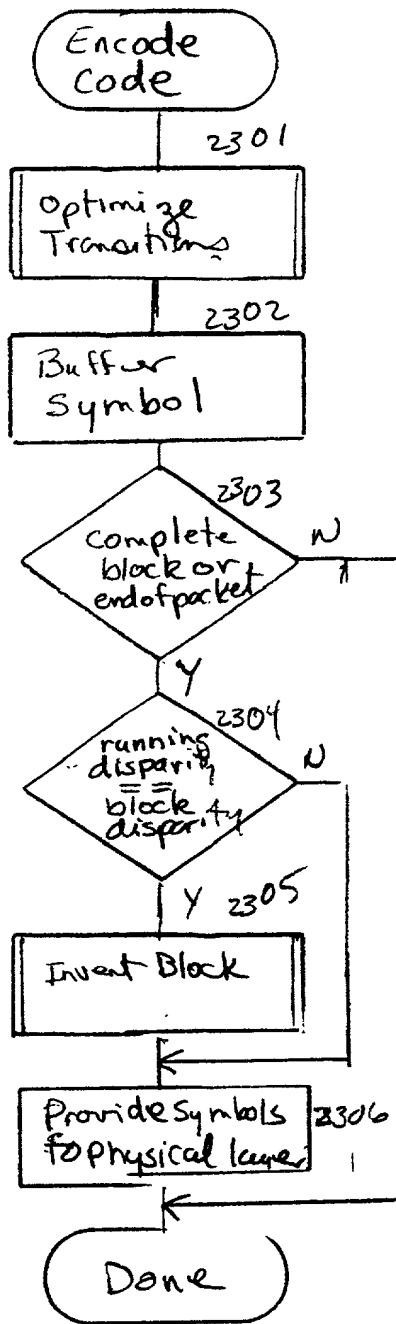


Fig 23

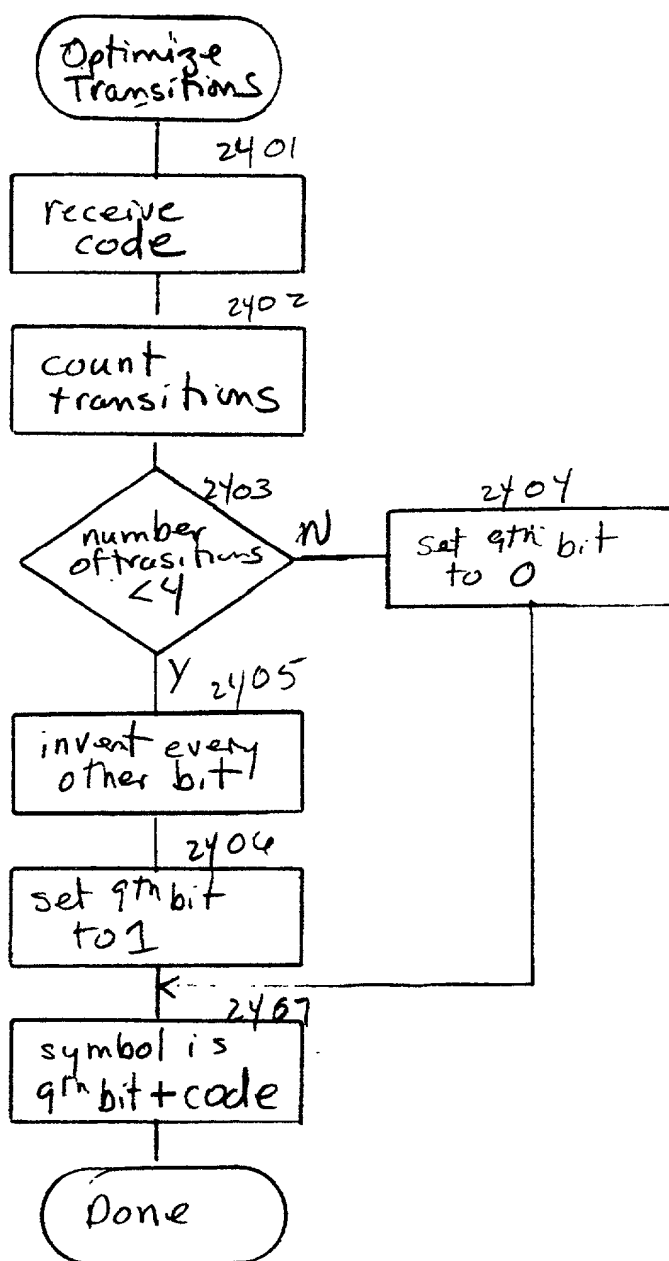


Fig 24

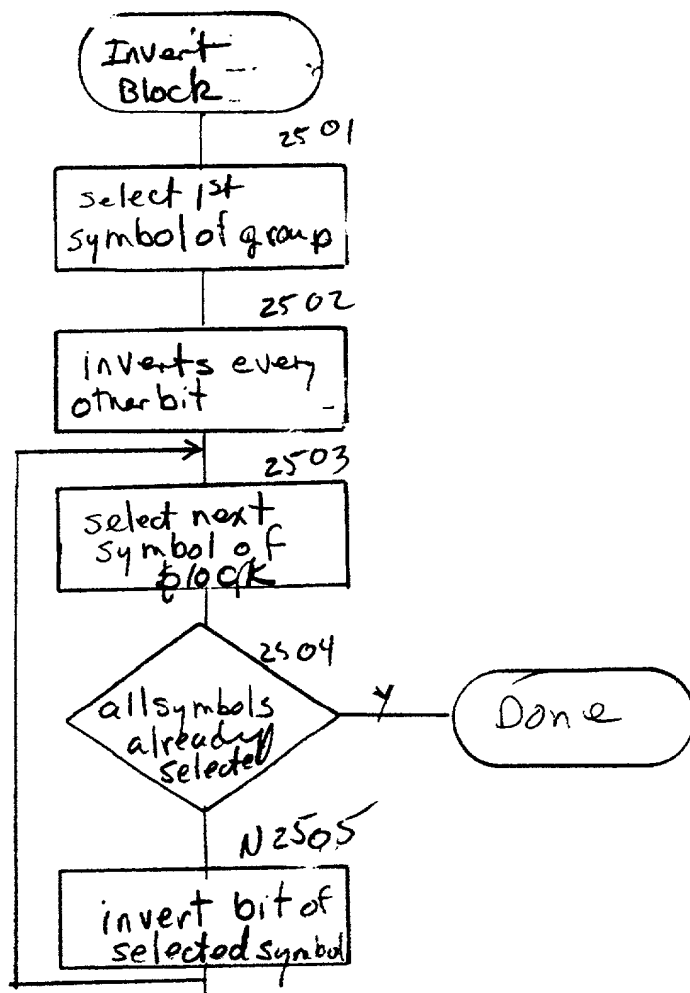


Fig 25

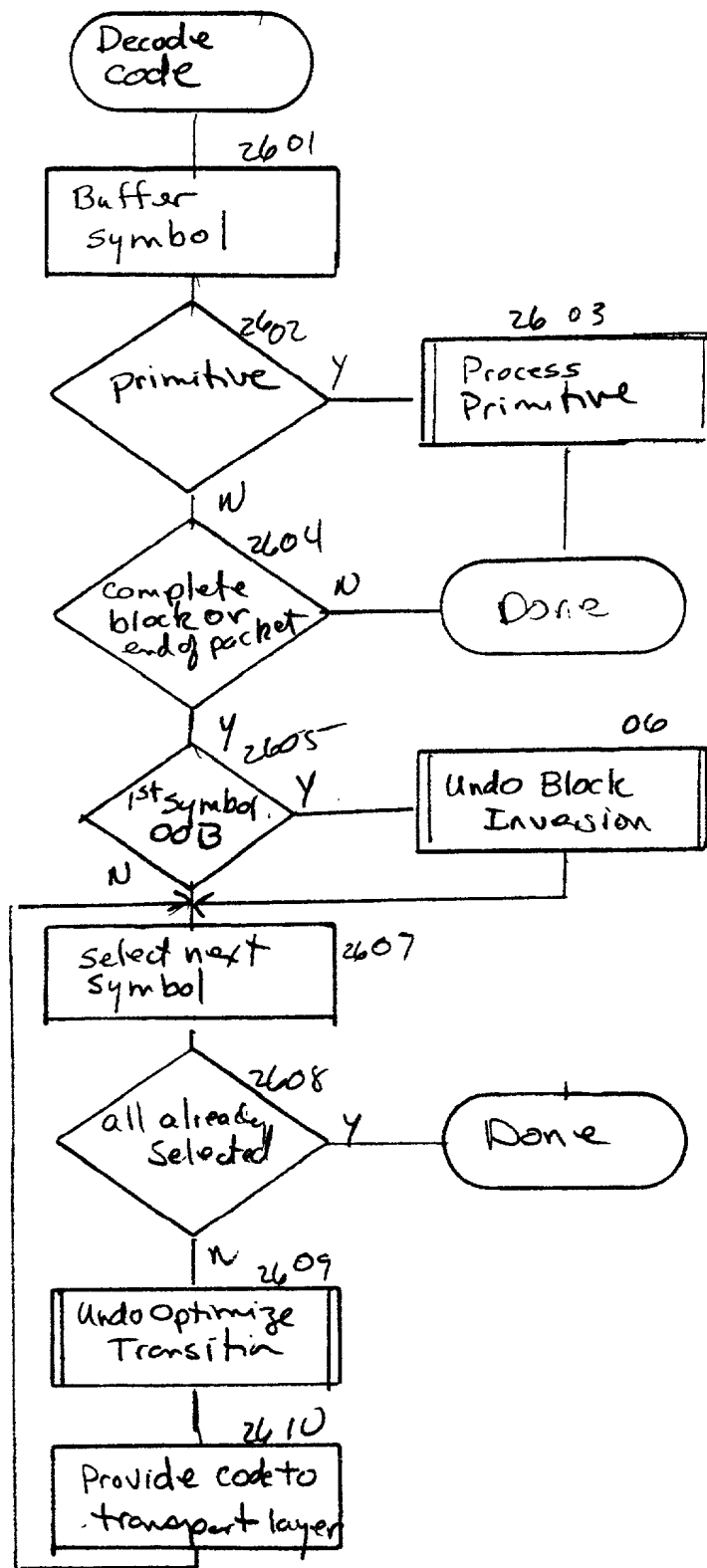


Fig 26

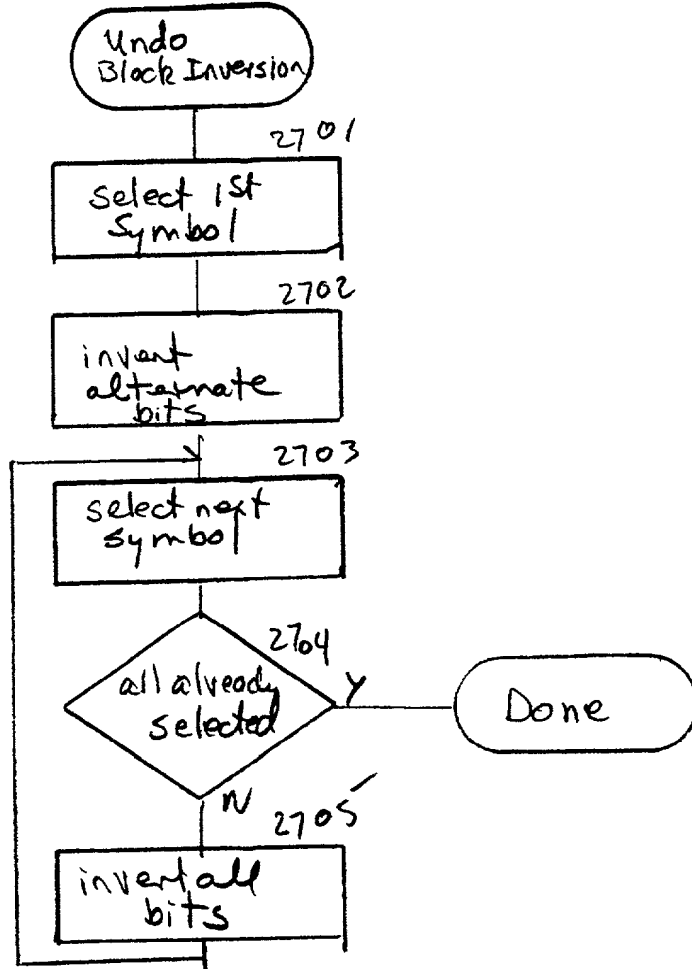


Fig 27

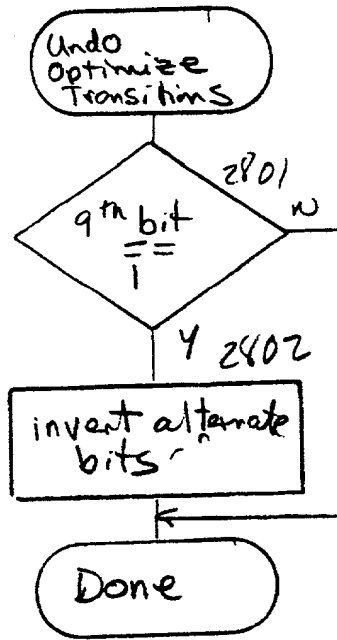


Fig 28

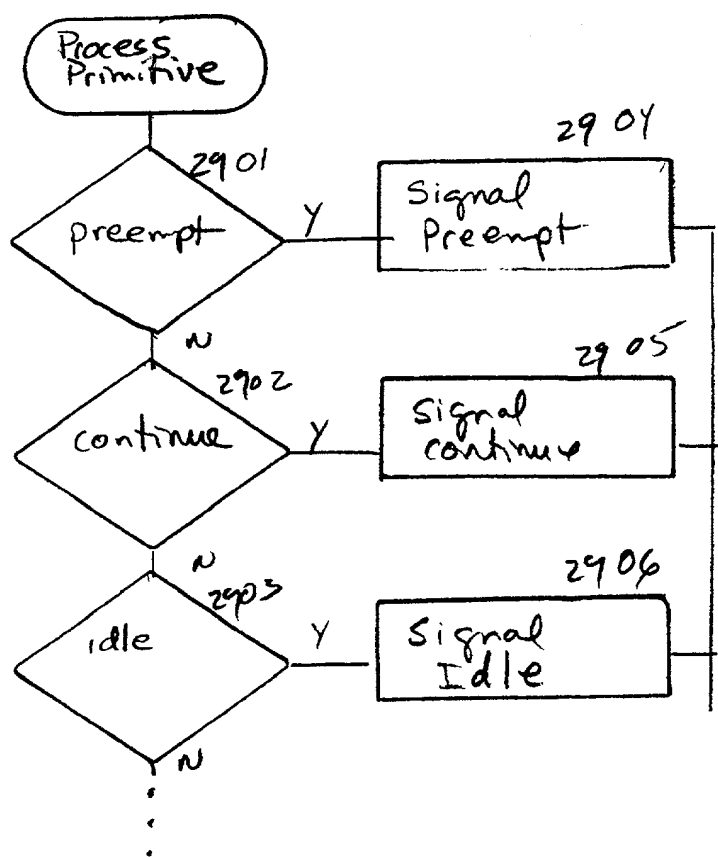


Fig 29

# Multiprot Memory Device 3000

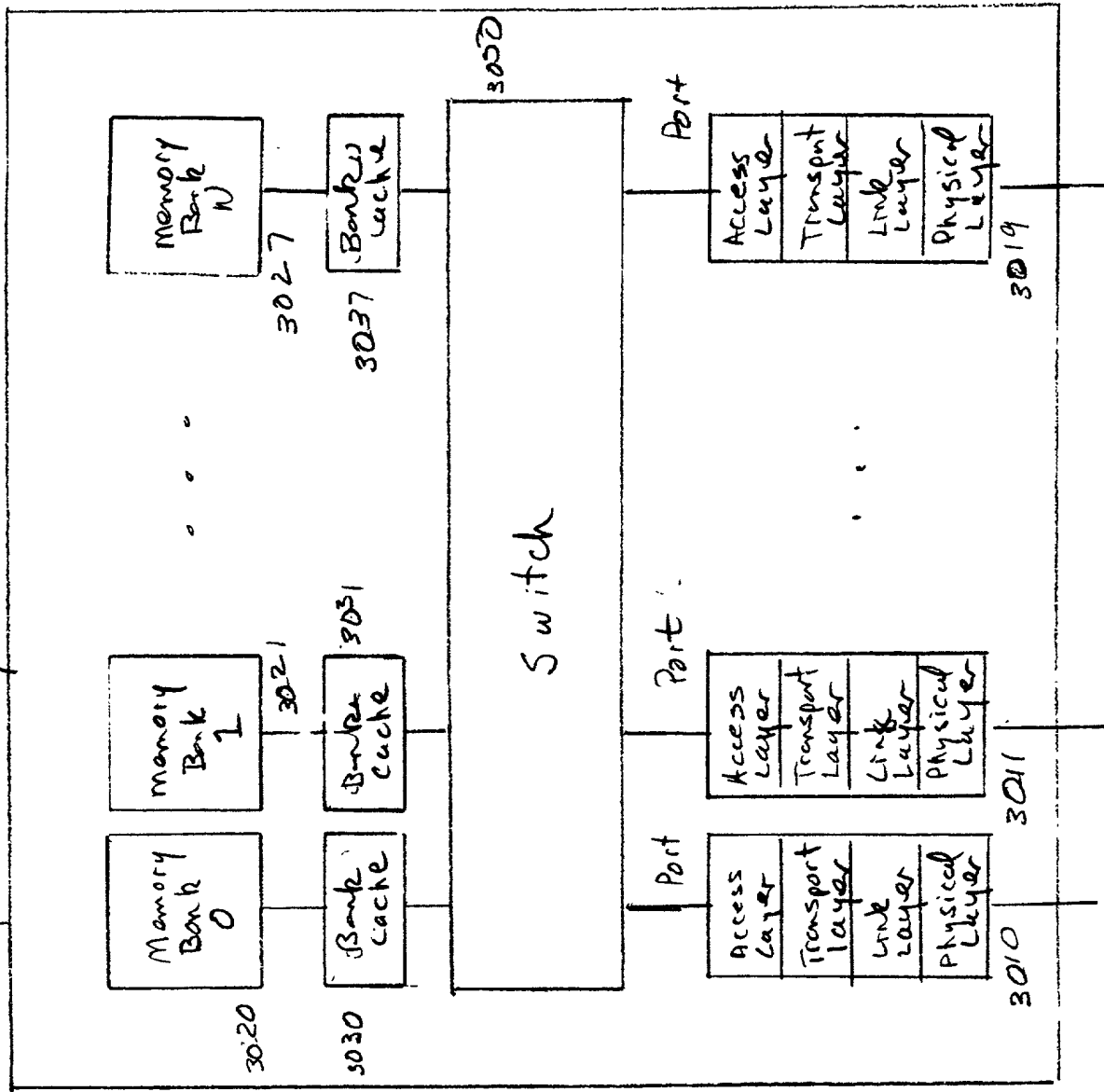
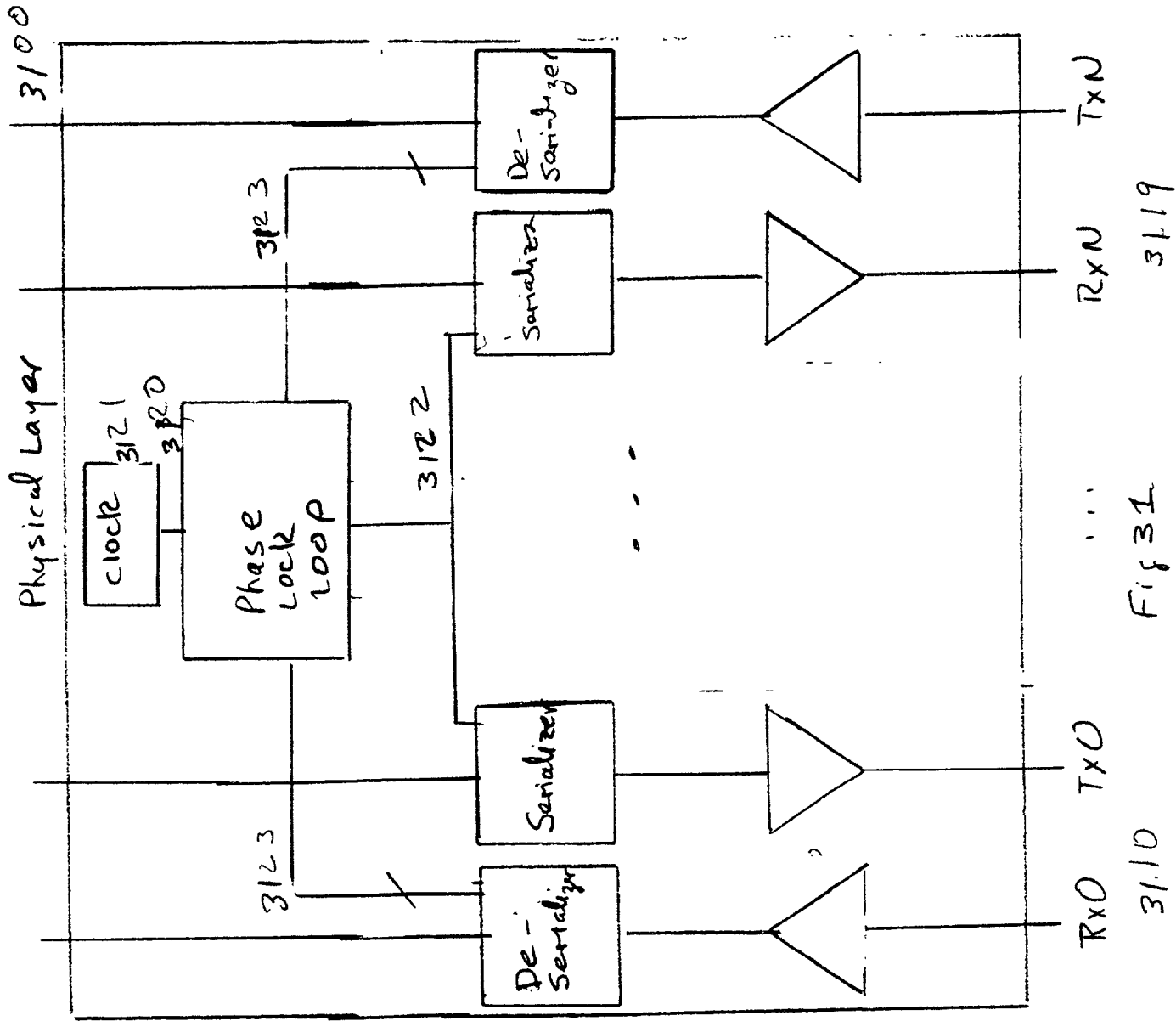


Fig 30



Input Queue 3201

Port	R/W	Address	Data
3	R	1000	
4	W	4000	10...1
3	W	1000	111...0
3	R	2000	
		...	

Output Queue 3202

Valid	Port	Data
1	3	11...0
0		
0		
1	3	101...1
	...	

Fig 32

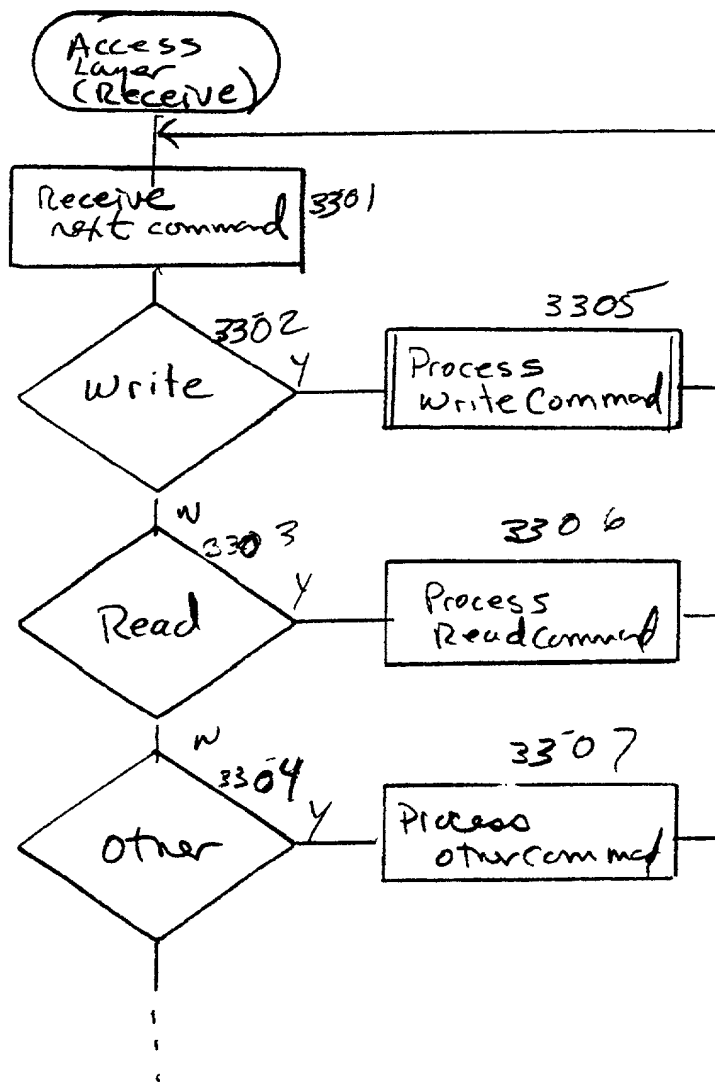


Fig 33

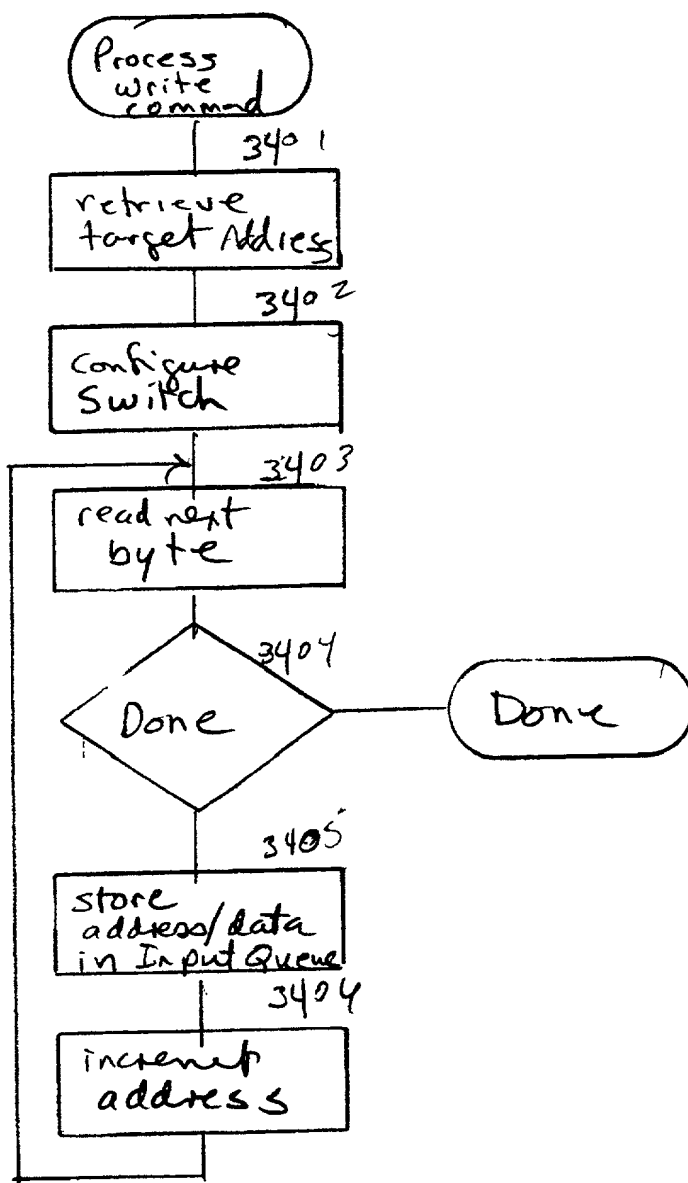


Fig 34

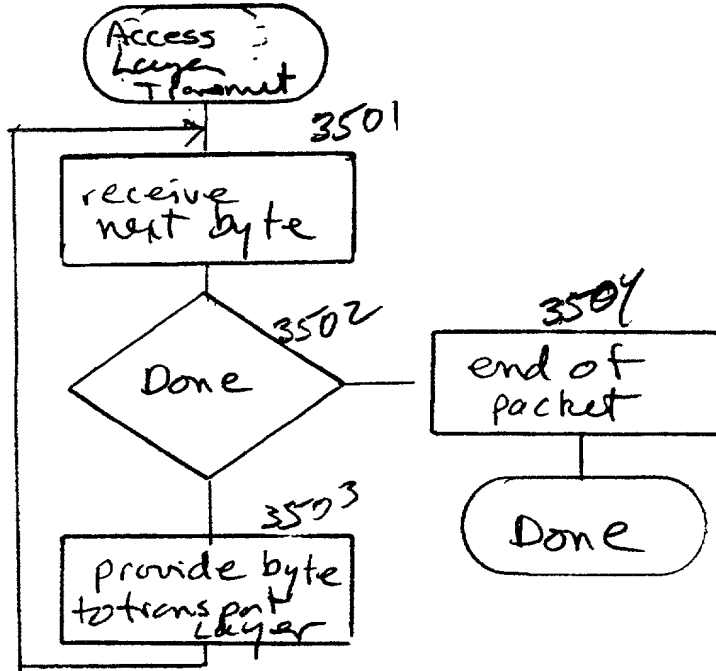


Fig 35

FIG. 36

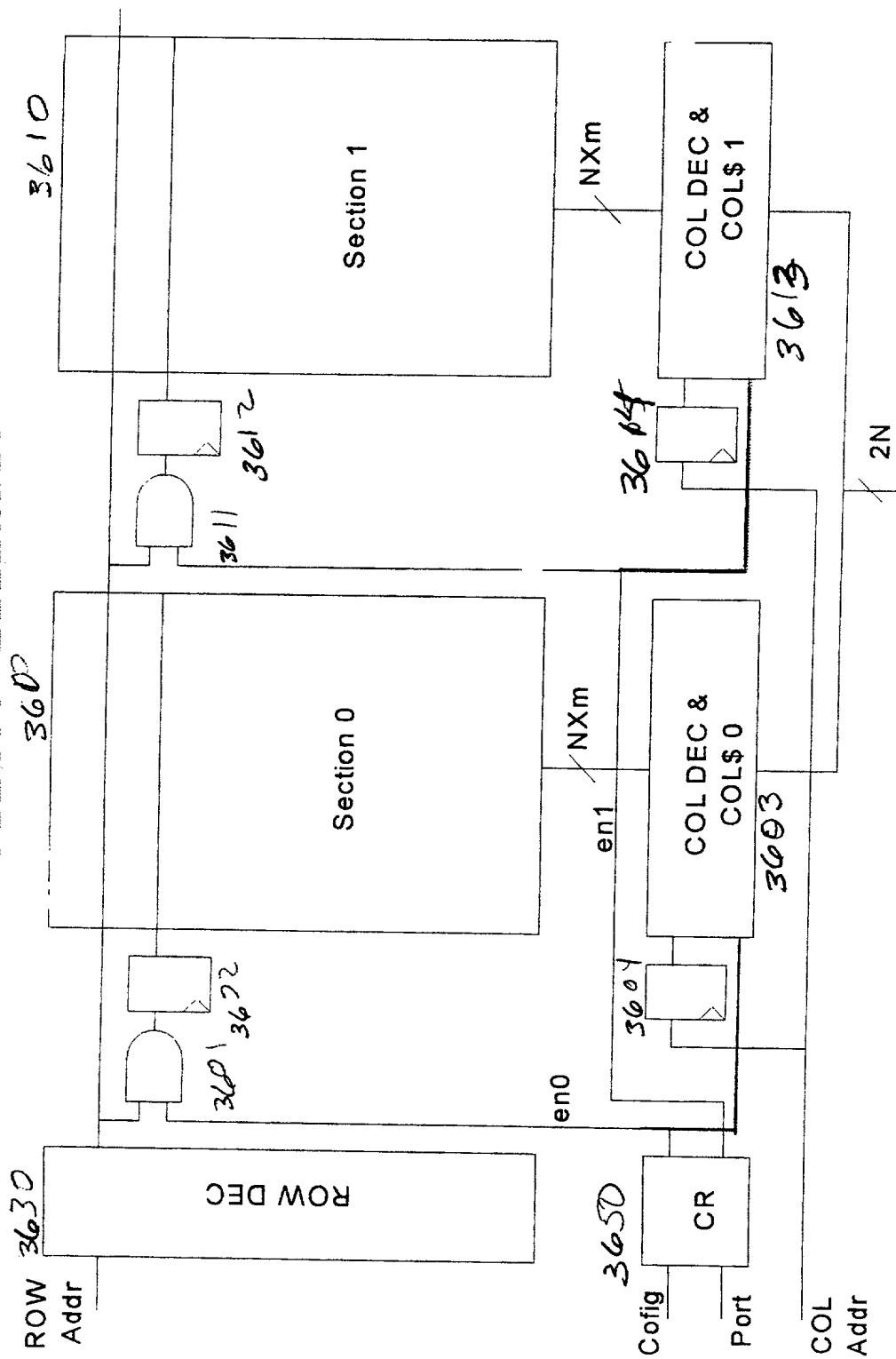
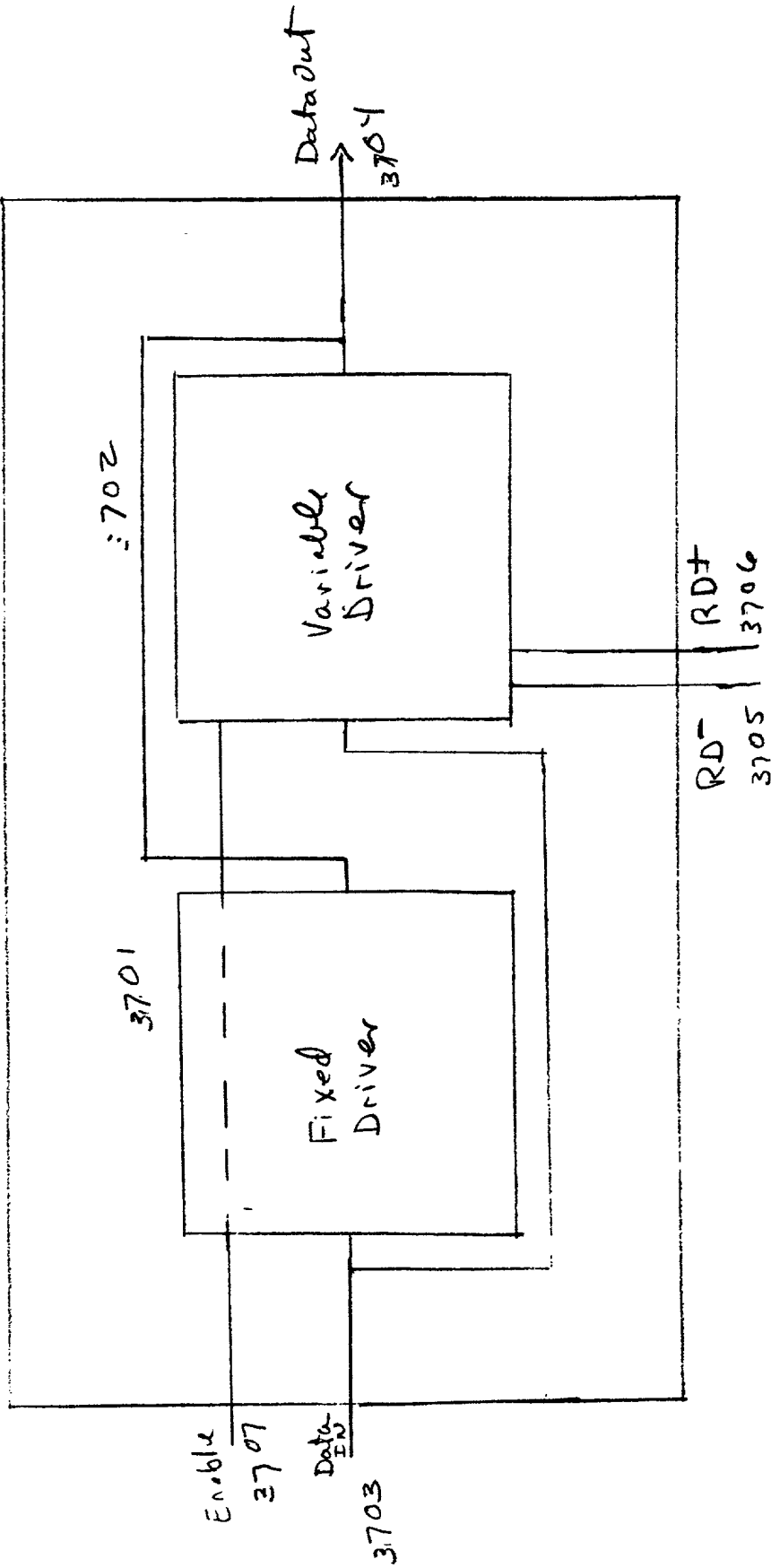


FIG. 36

# Line Driver 3700



Variable Driver

$$\begin{cases} RD^+ \wedge \overline{DataIn} = \text{pull down} \\ RD^- \wedge DataIn = \text{pull up} \end{cases}$$

Fig 37A

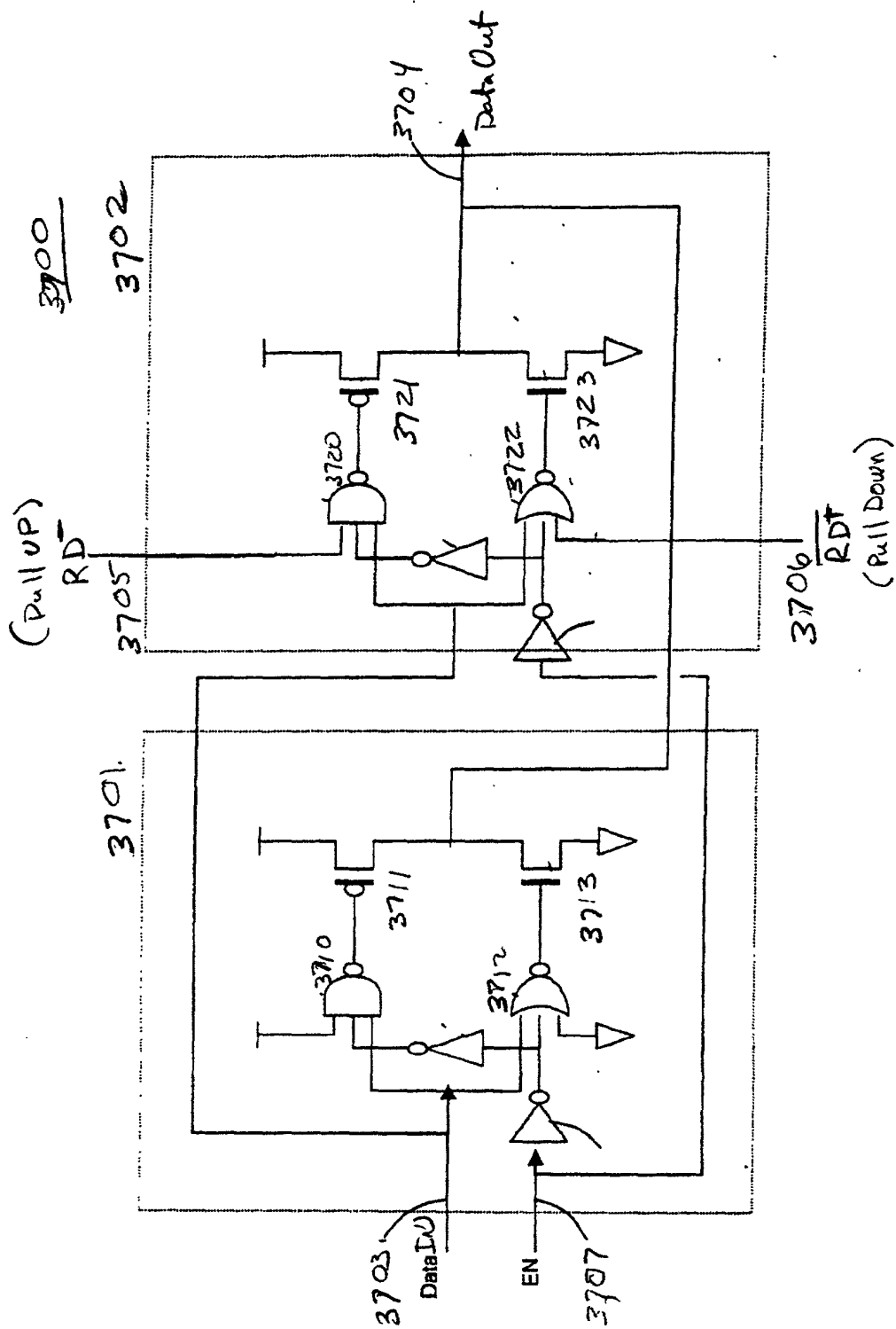
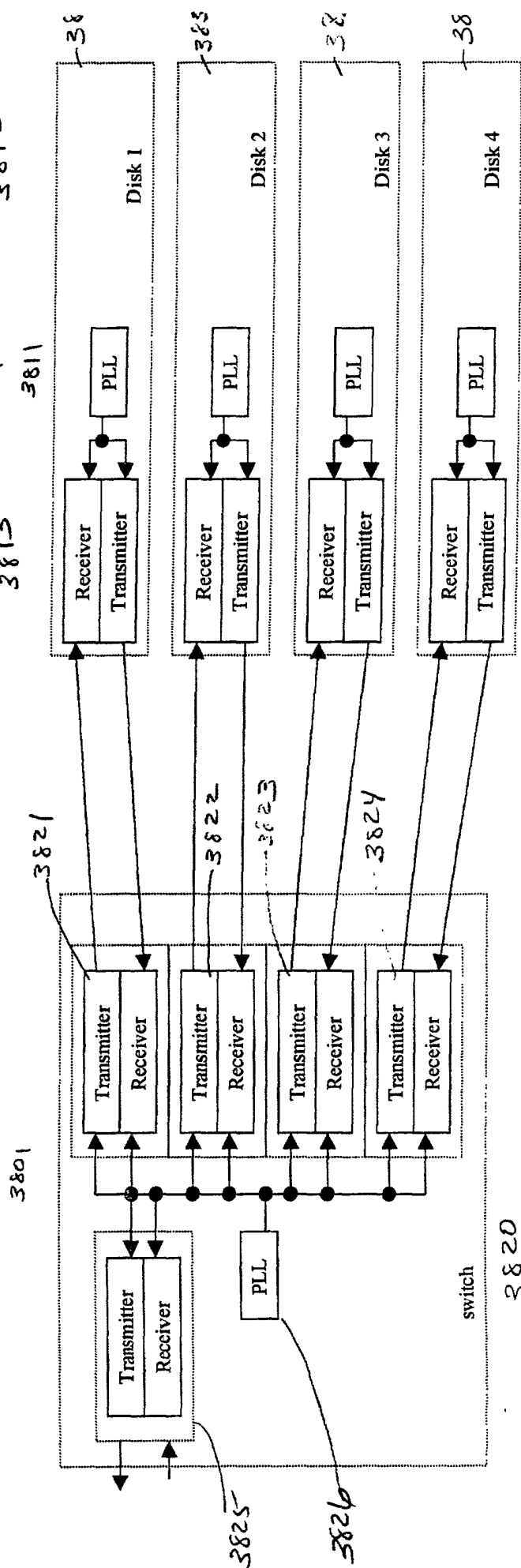
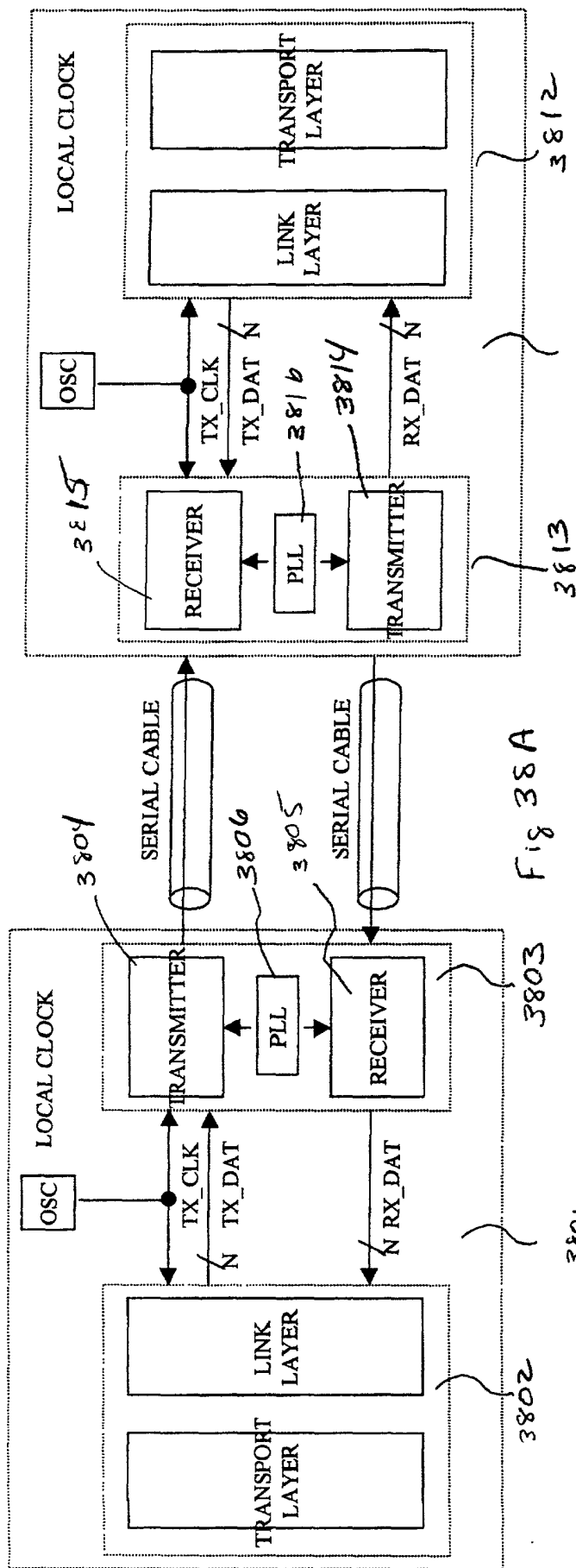


Fig 37B



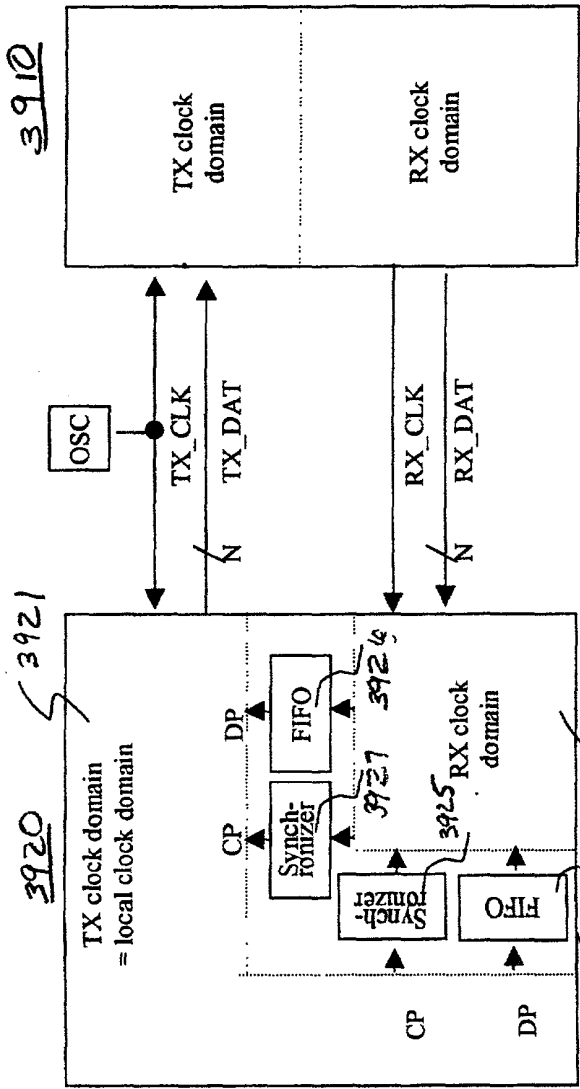


Fig 39A

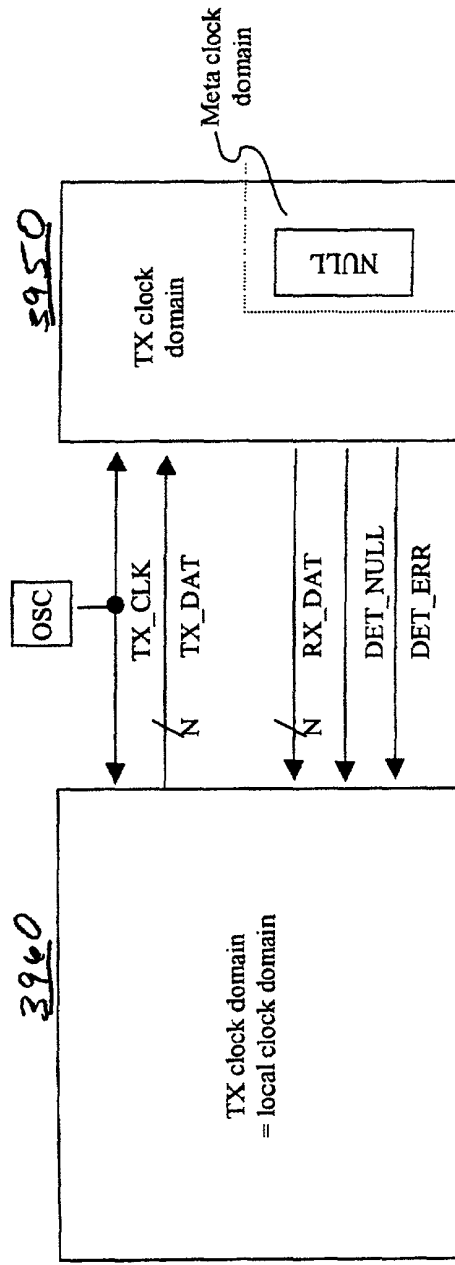


Fig 39B

Serial storage channel

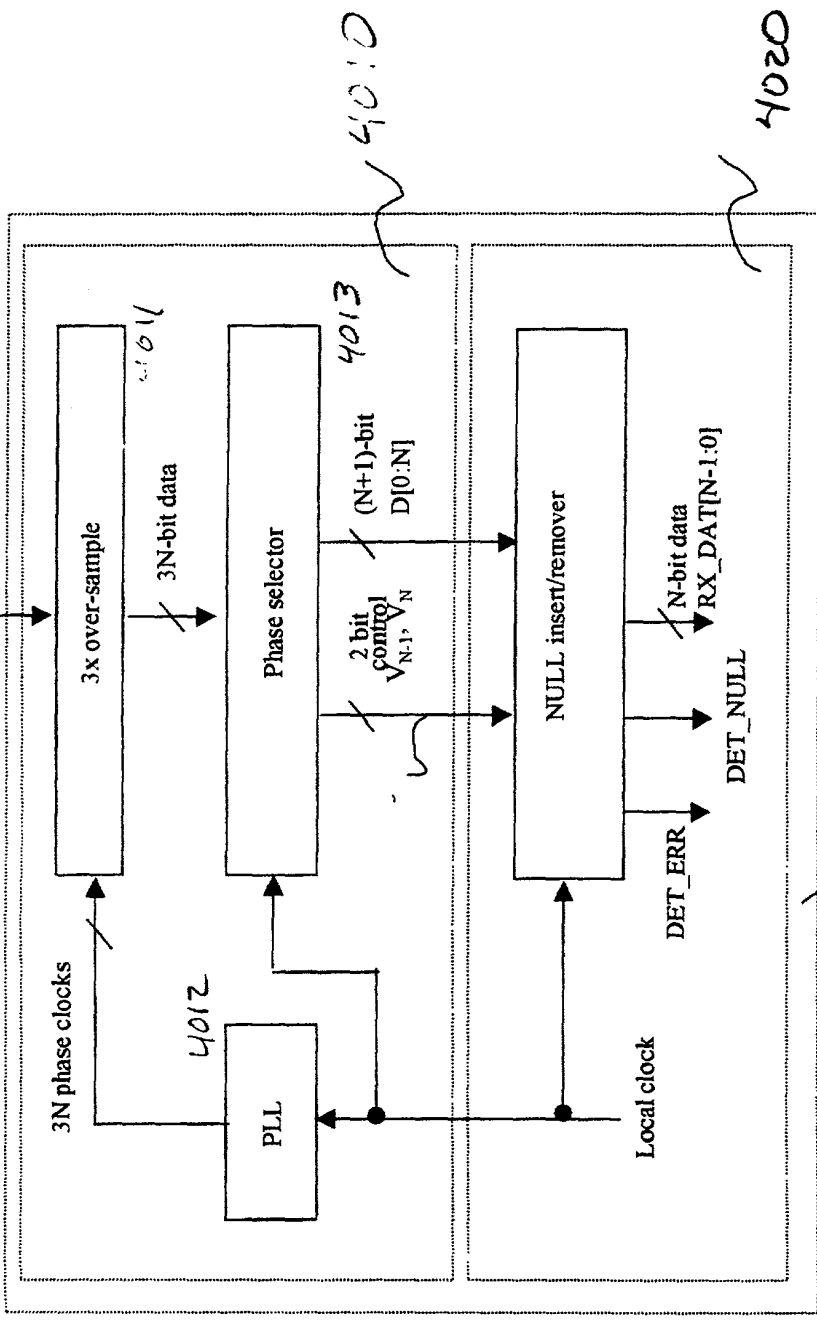


Fig 40

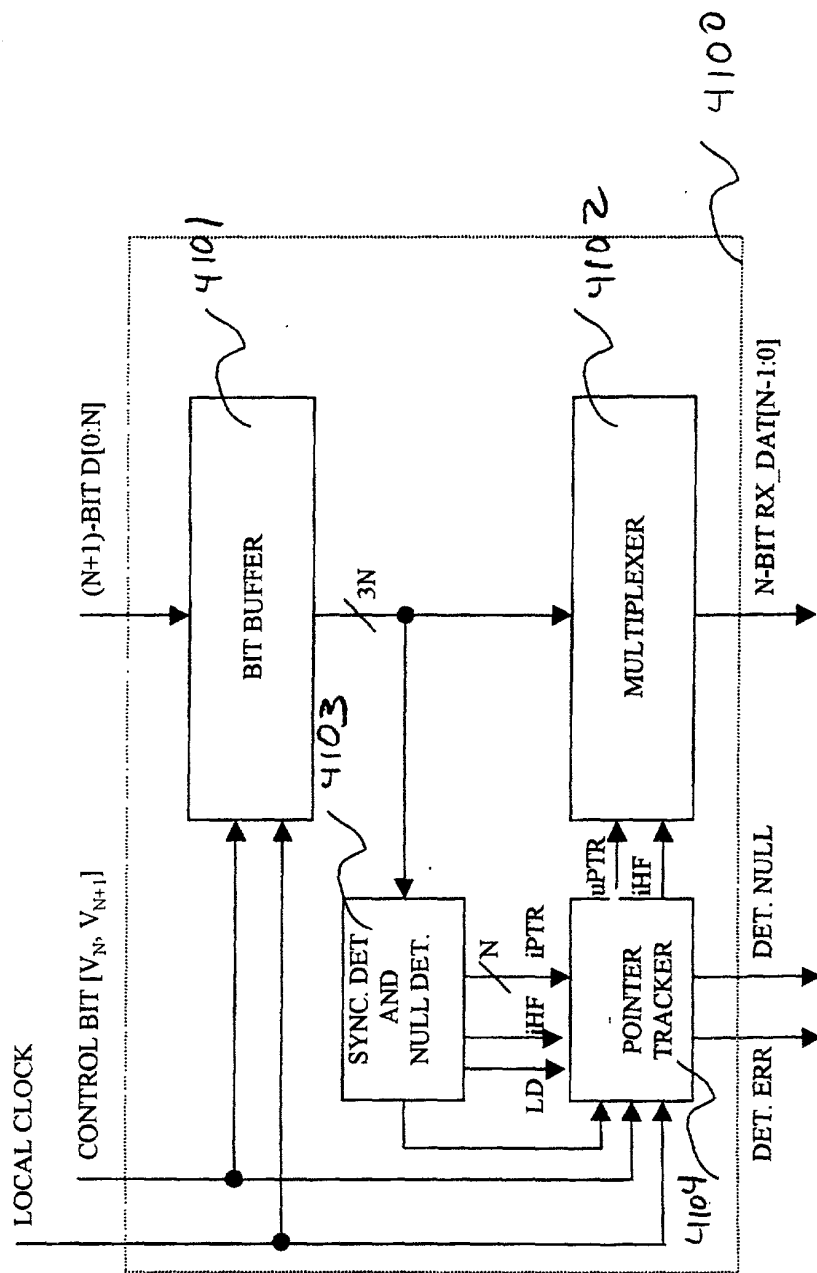


Fig 41

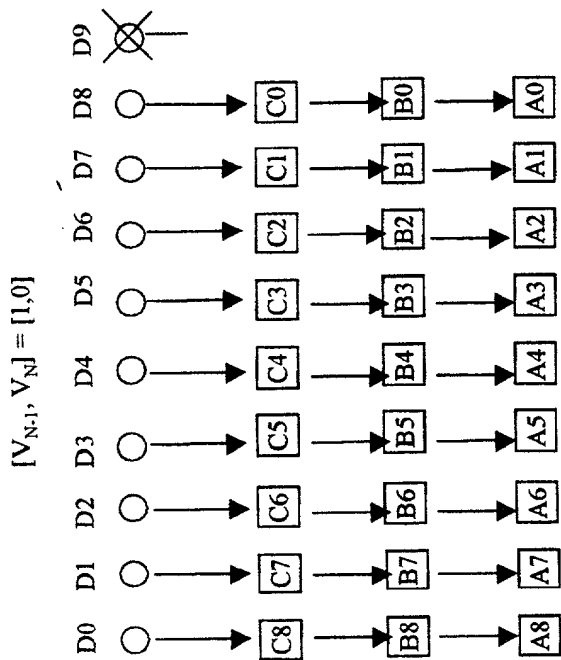


Fig. 42A

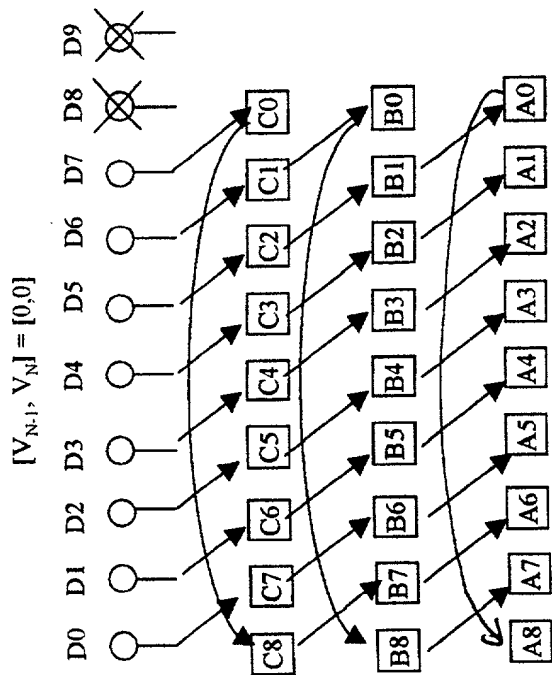


Fig 42 B

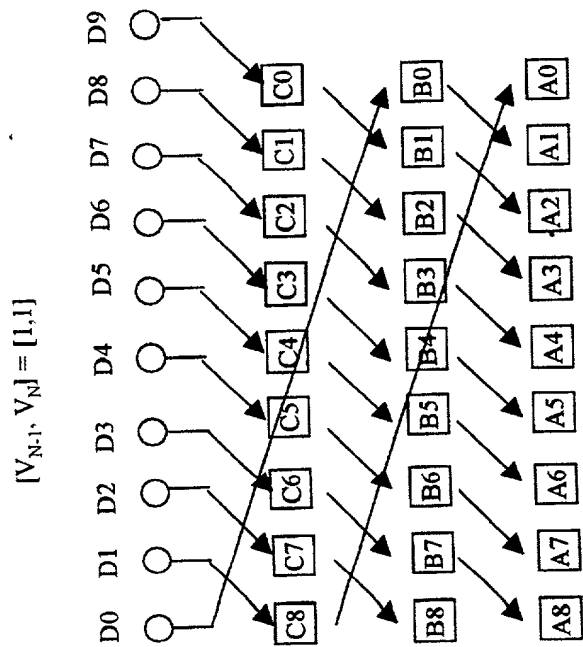


Fig 42c

FIG. 43 is a block diagram of a system for processing a half line of data.

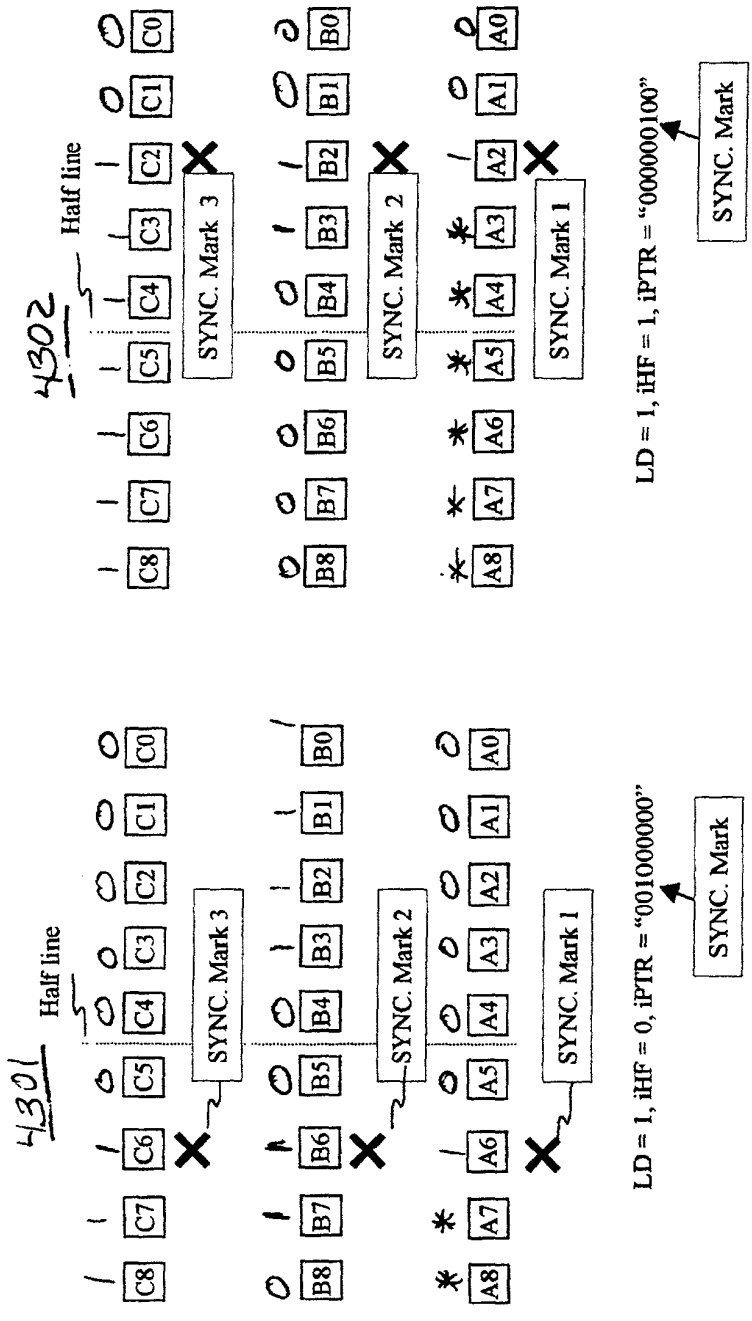
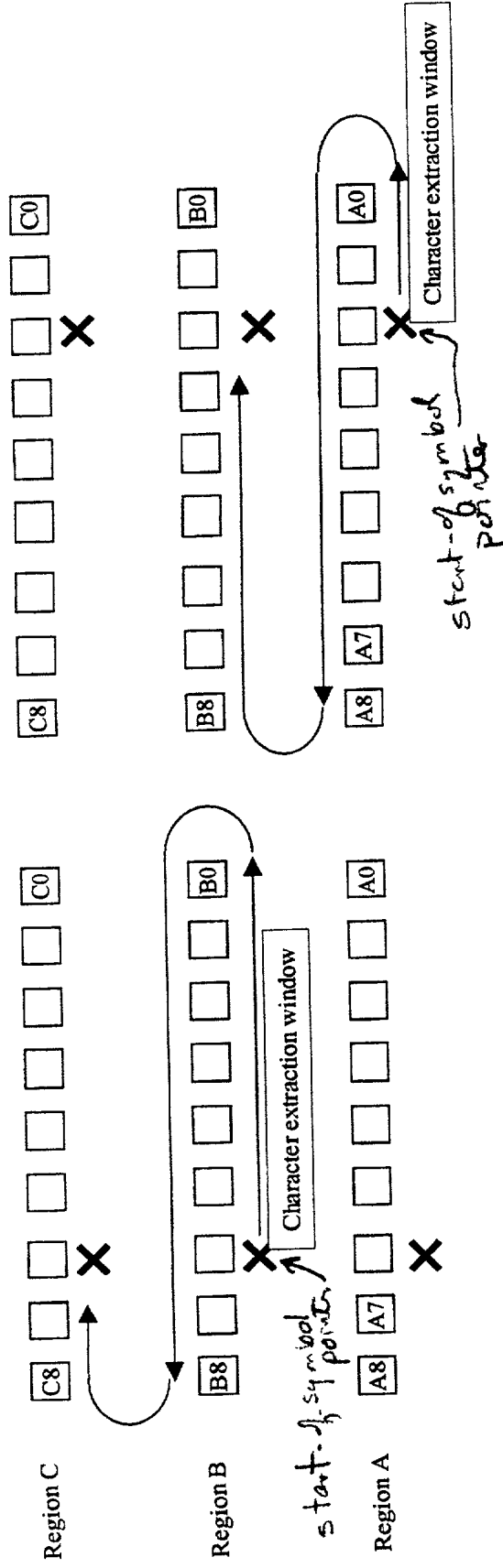


Fig. 43



LD = 1, iHF = 1, iPTR = "000000100"

LD = 1, iHF = 0, iPTR = "0010000000"

Fig 44

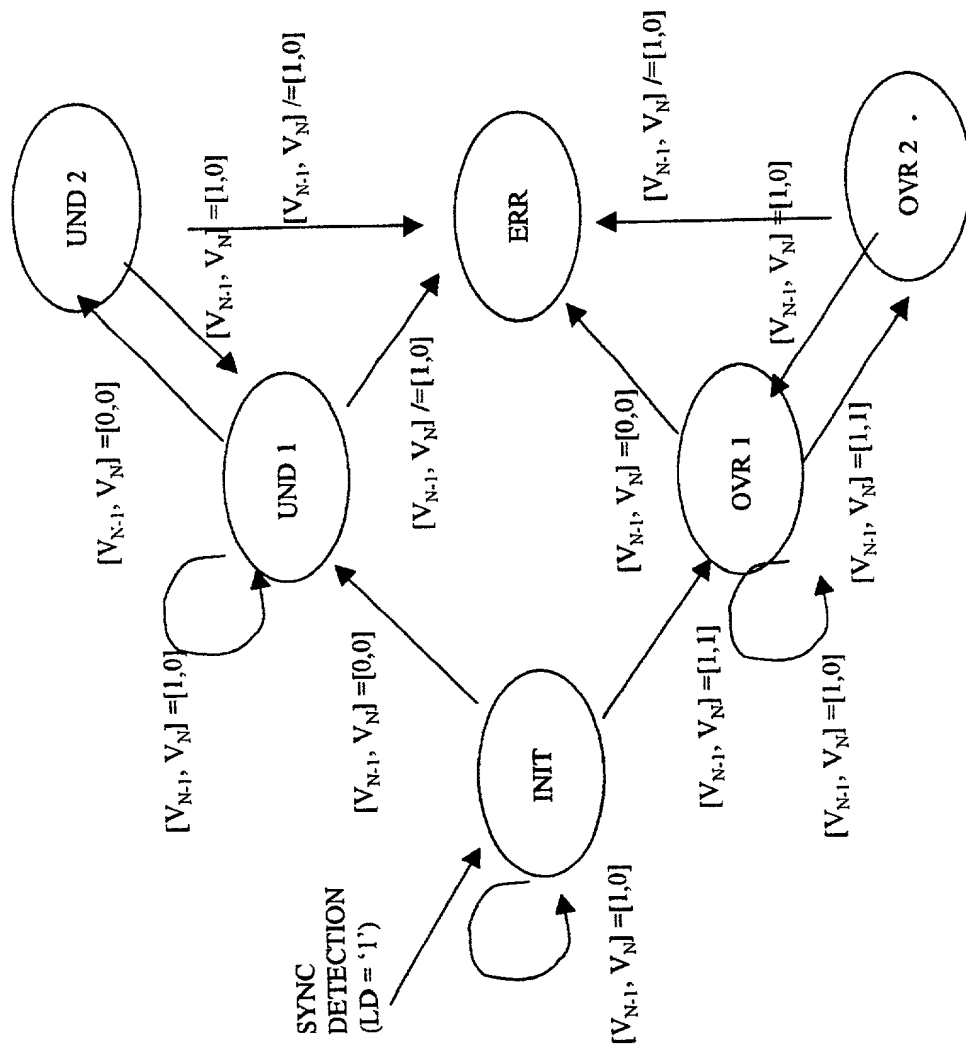


Fig 45

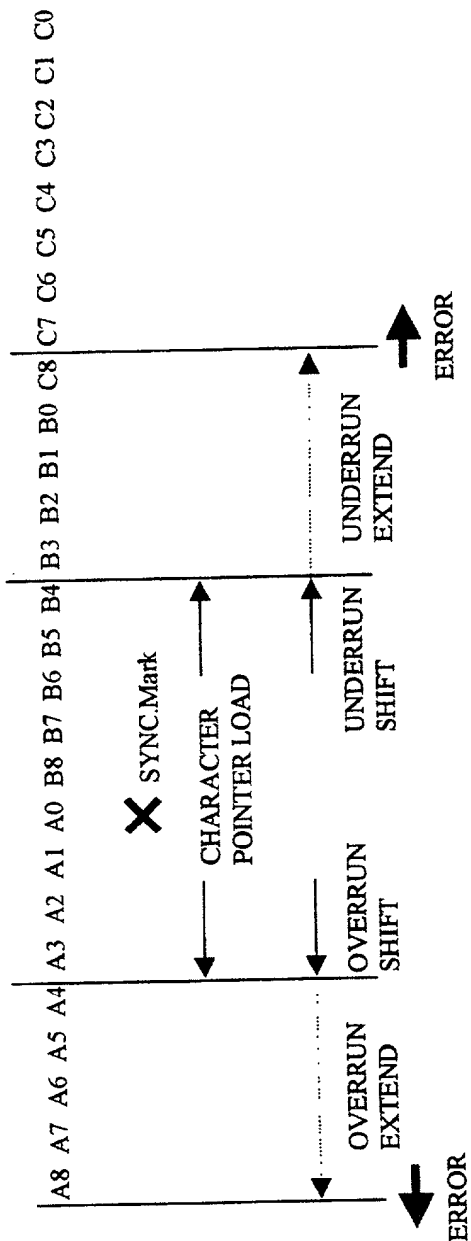


Fig 46

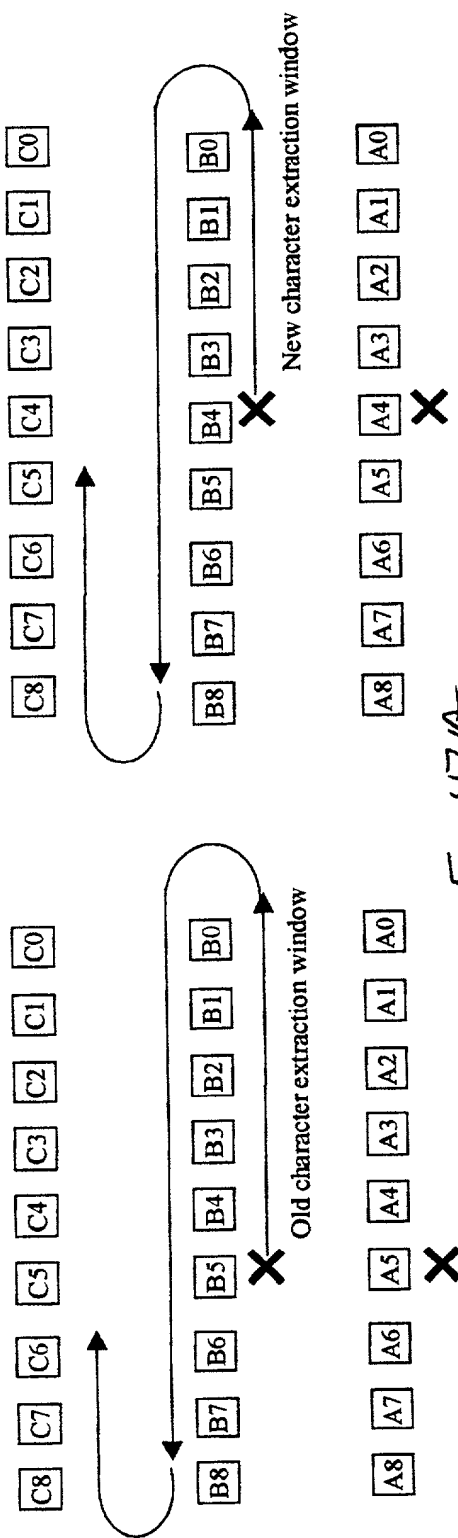


Fig 47A

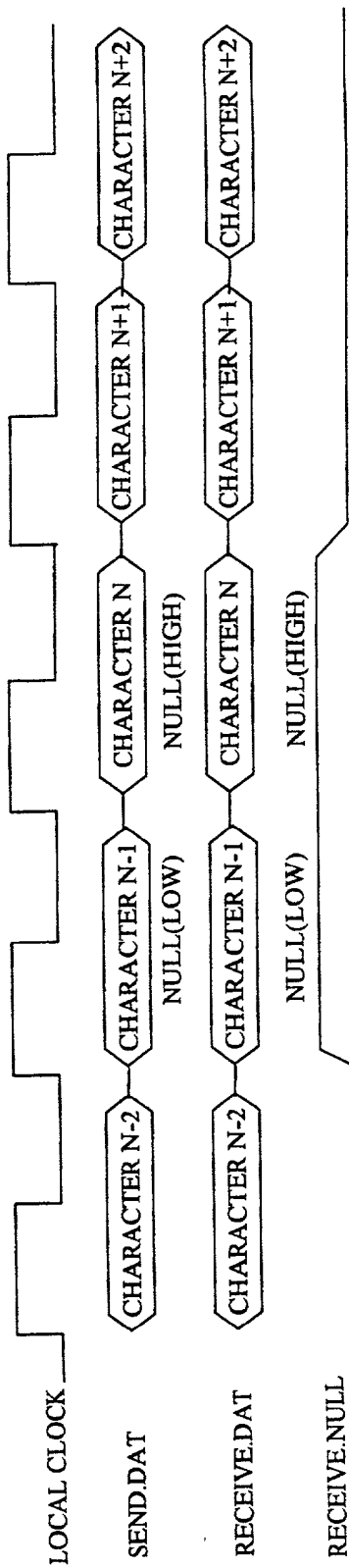


Fig 47B

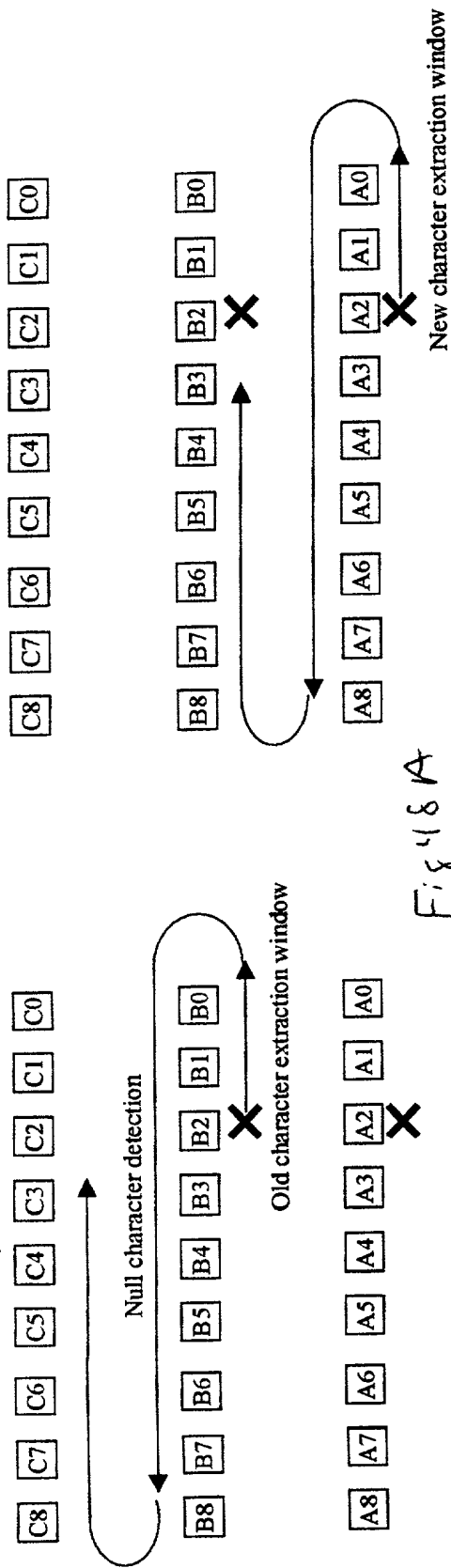


FIG. 48A

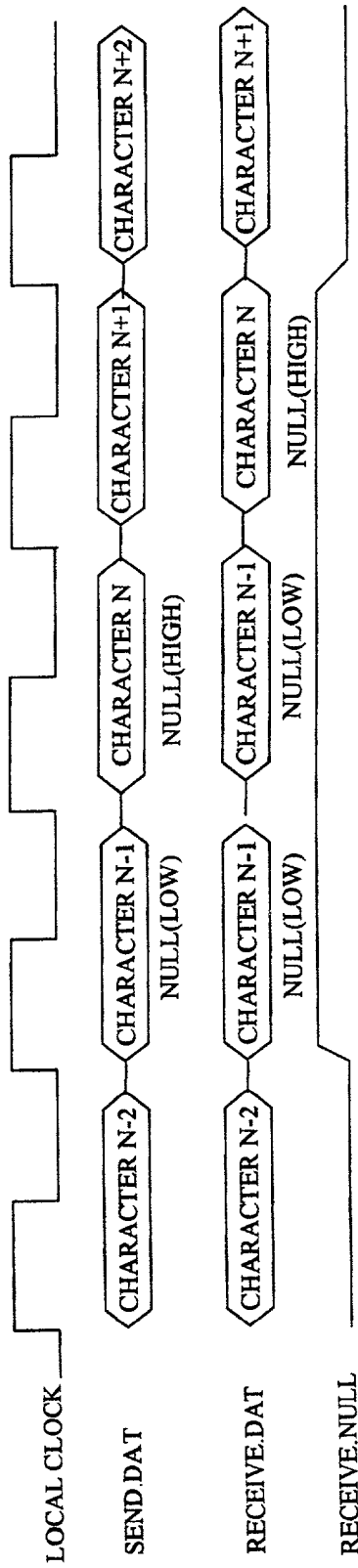


Fig 48B

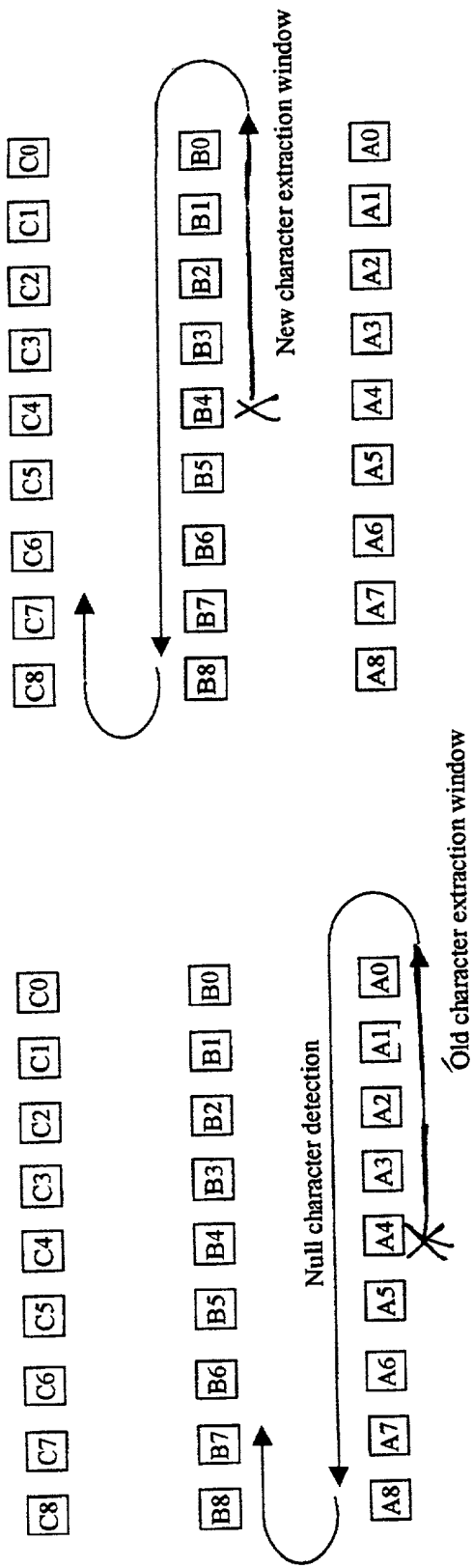


Fig. 49A

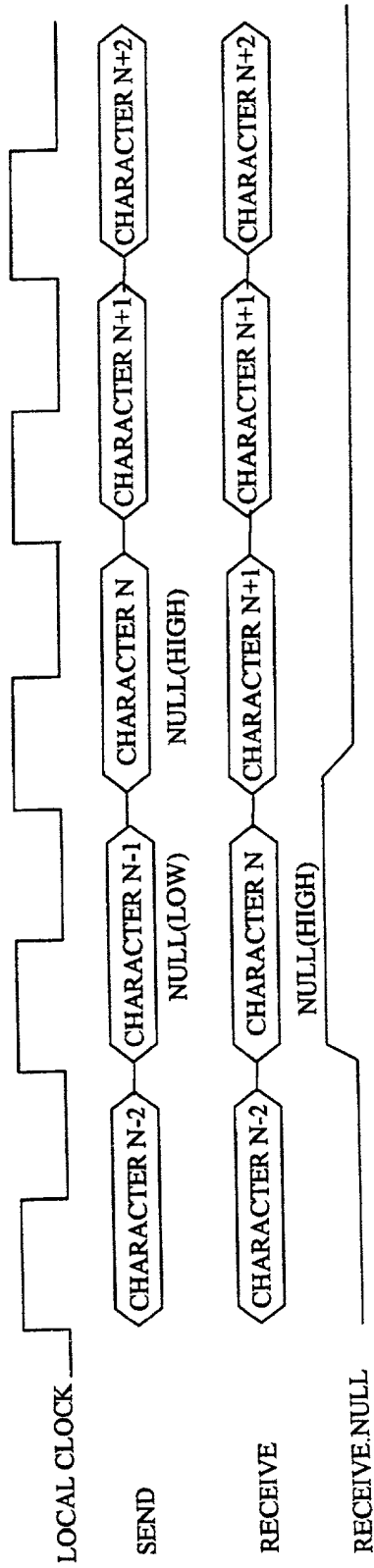


Fig 49B